GOSTONE

RoHS COMPLIANT

GTD1209A

Dual N-channel Power MOSFET:
12V, 0.9mohm, 38A

Product Summary

VSSS	VGSS	RSS(ON) TYP/MAX	IS MAX
12V	± 8V	0.85/1.15mΩ@VGS=4.5V 0.90/1.20mΩ@VGS=3.8V 1.15/1.70mΩ@VGS=3.1V 1.55/3.00mΩ@VGS=2.5V	38A

Features

- ❖CSP (Chip Size Package)
- ❖Halogen-Free / RoHS Compliant
- ❖2.5V Drive Low Source-Source On-State Resistance
- ❖Gate Resistor Installed Common-Drain Type MOSFET
- ❖ESD Protection Diode Installed (Gate-Source)

Application

- ❖ Lithim-Ion Secondary Battery Protection Circuits

Form

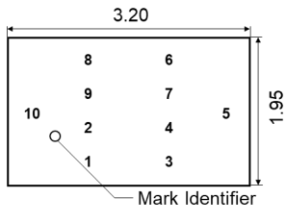
- ❖ Tape & Reel Embossed Type: 5,000pcs / reel

Absolute Maximum Rating (Ta=25°C)

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	12	V
Gate-source Voltage		VGS	± 8	V
Source Current	DC *1	IS1	22.7	A
	DC *2	IS2	38.0	
	DC *3	IS3	54.0	
	Pulsed *4	ISp	227	
Total Power Dissipation	DC *1	PD1	0.62	W
	DC *2	PD2	1.80	
	DC *3	PD3	3.50	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

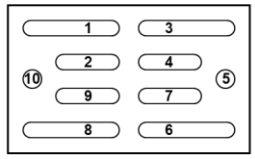
Unit: mm

(Top View)



(Front View)

(Bottom View)



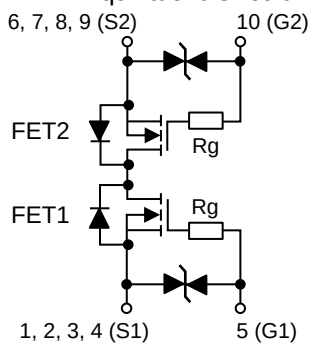
1, 2, 3, 4. Source1 (FET1) 5. Gate1 (FET1)
6, 7, 8, 9. Source2 (FET2) 10. Gate2 (FET2)

Thermal Characteristic (Ta=25°C)

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	202	°C / W
	Rth2 *2	70	
	Rth3 *3	36	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (62 mm^2 area, 36 µm thickness).
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (612 mm^2 area, 36 µm thickness).
*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
*4 t = 10 µs, Duty Cycle ≤ 1 %.

Equivalent Circuit



Electrical characteristics (Ta=25°C ± 3°C)

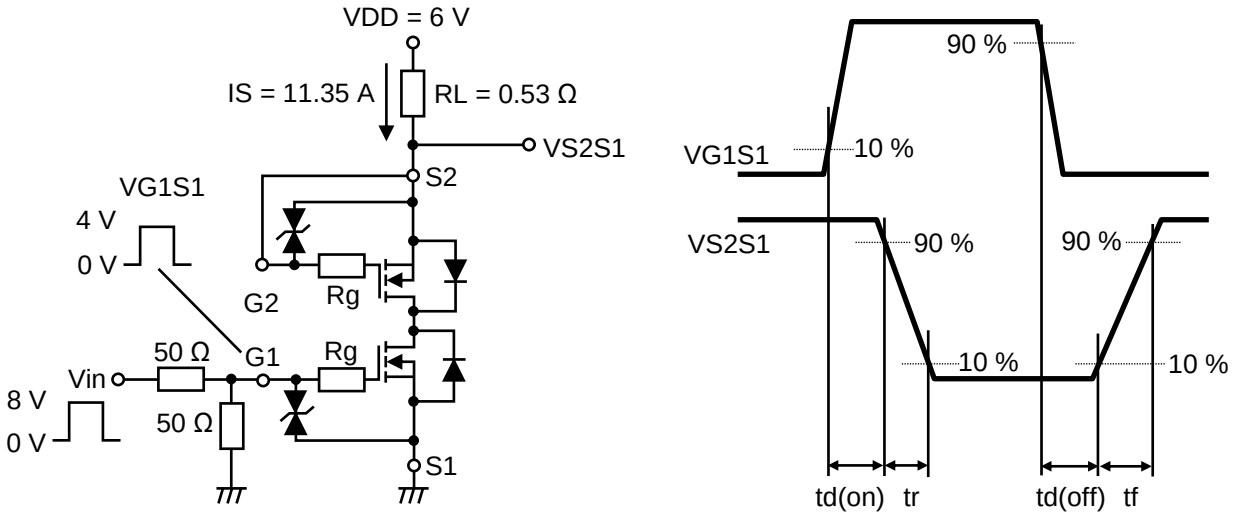
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 10	μA
	IGSS2	VGS = ± 5 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 1.1 mA, VSS = 6 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 11.35 A, VGS = 4.5 V	0.60	0.85	1.15	mΩ
	RSS(on)2	IS = 11.35 A, VGS = 3.8 V	0.60	0.90	1.20	
	RSS(on)3	IS = 11.35 A, VGS = 3.1 V	0.70	1.15	1.70	
	RSS(on)4	IS = 11.35 A, VGS = 2.5 V	0.95	1.55	3.00	
Body Diode Forward Voltage	VF(s-s)	IF = 11.35 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		8050		pF
Output Capacitance *1	Coss			1100		
Reverse Transfer Capacitance *1	Crss			1000		
Turn-on Delay Time *1, *2	td(on)	VDD = 6 V, VGS = 0 to 4 V		2.4		μs
Rise Time *1, *2	tr	IS = 11.35 A		3.8		
Turn-off Delay Time *1, *2	td(off)	VDD = 6 V, VGS = 4 to 0 V		14.0		μs
Fall Time *1, *2	tf	IS = 11.35 A		7.0		
Total Gate Charge *1	Qg	VDD = 6 V		70		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		17		
Gate-drain Charge *1	Qgd	IS = 22.7 A		14		
Gate Resistance *1	Rg	f = 1 MHz	400	700	1000	Ω

Note:

*1 Guaranteed by design, not subject to production testing.

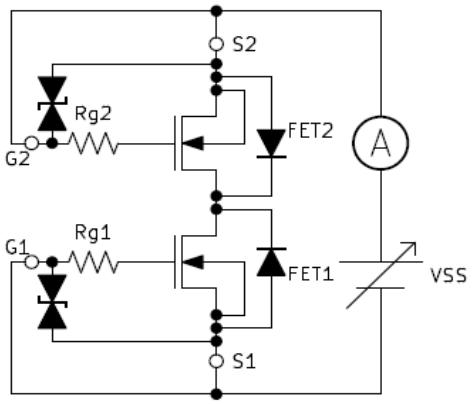
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

FET1 Measurement Circuit for Switching Characteristics td(on), tr, td(off), tf (FET2: Gate-Source Short)

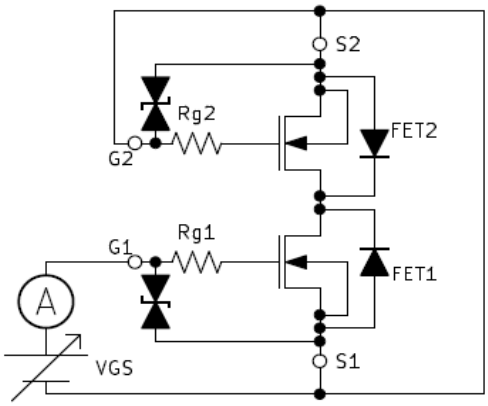


Test Circuit for FET1

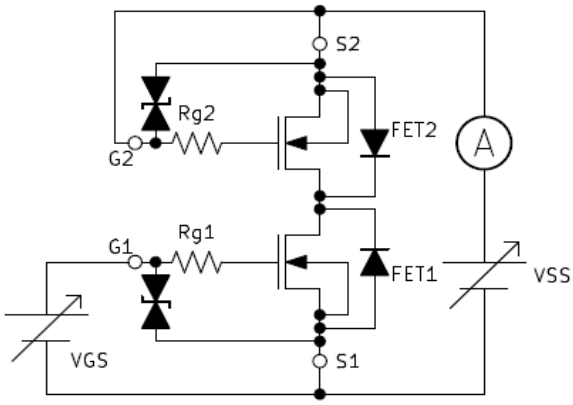
Test Circuit 1
VGSS/ISSS



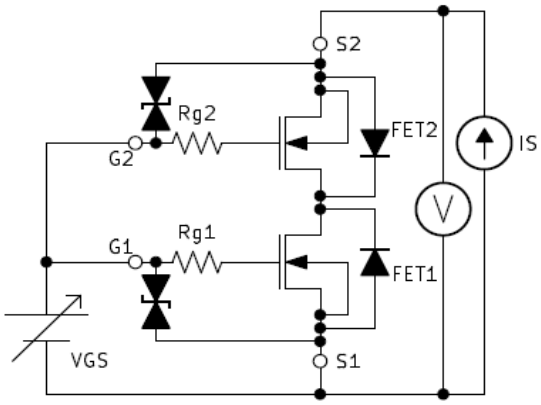
Test Circuit 2
IGSS/1/2



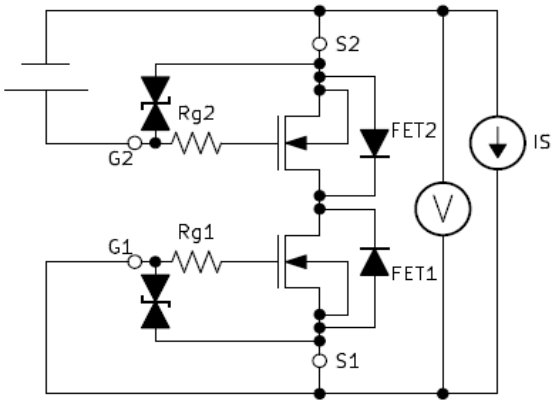
Test Circuit 3
Vth



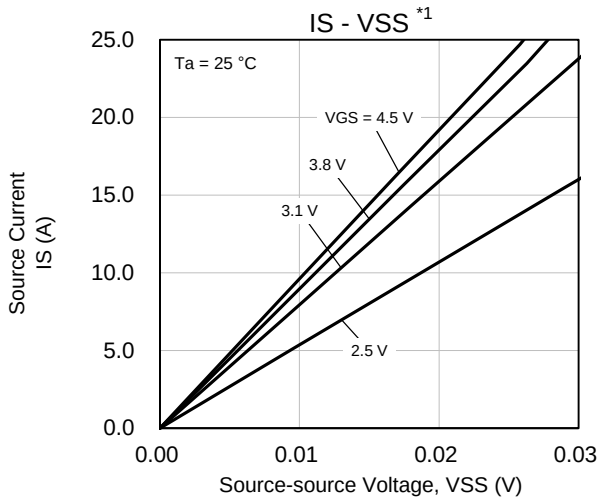
Test Circuit 4
RSS(on)

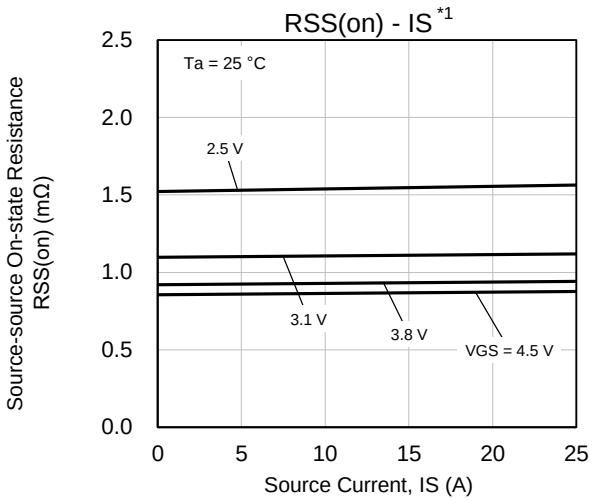


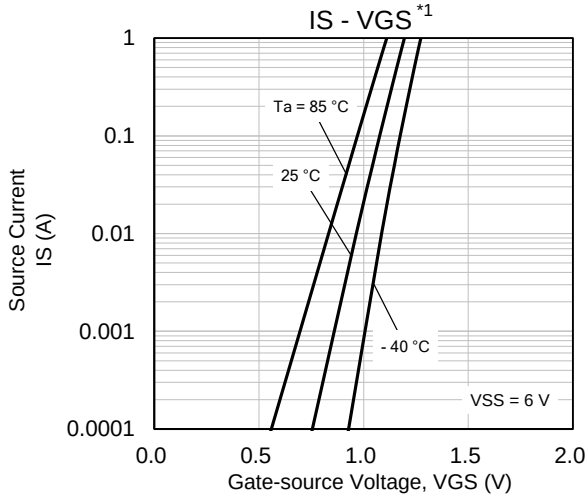
Test Circuit 5
VF(S-S)

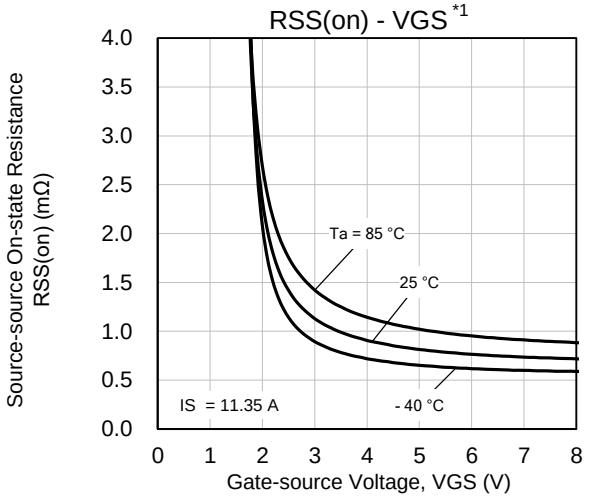


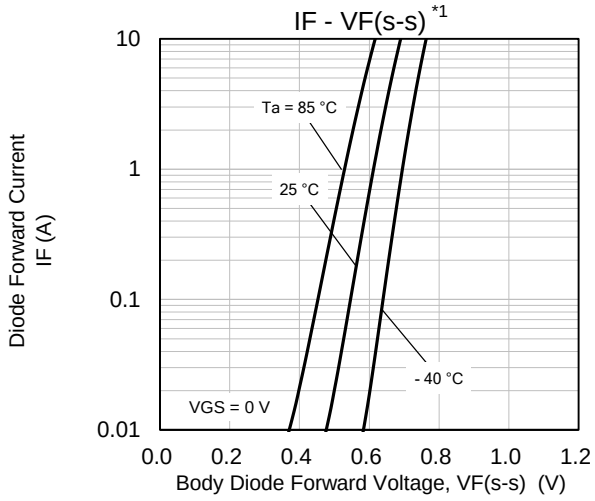
Technical data

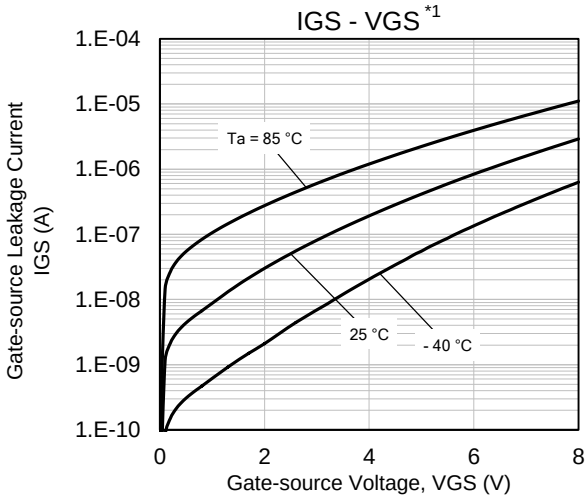






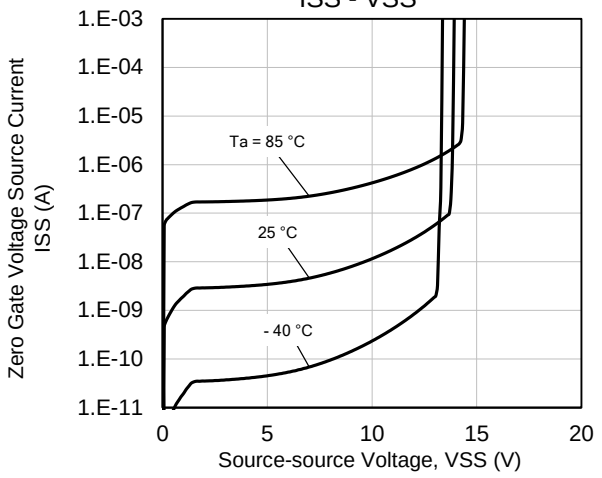




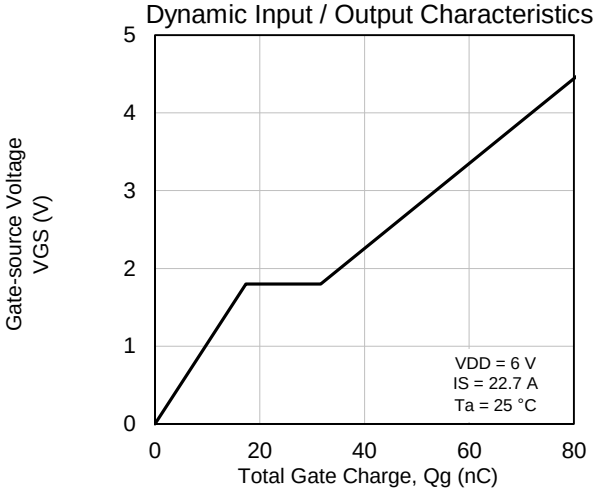


Technical data

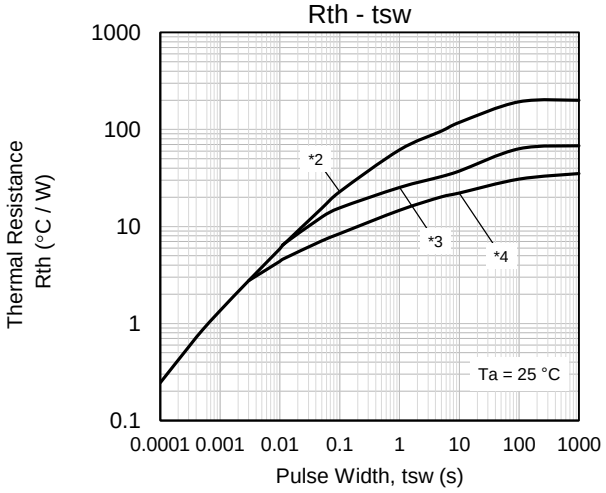
ISS - VSS *1



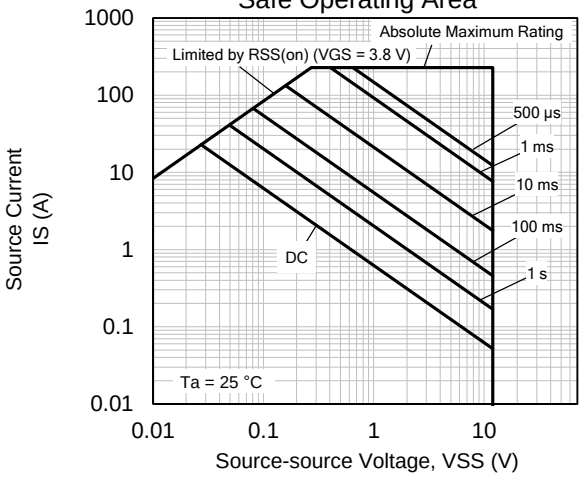
Dynamic Input / Output Characteristics



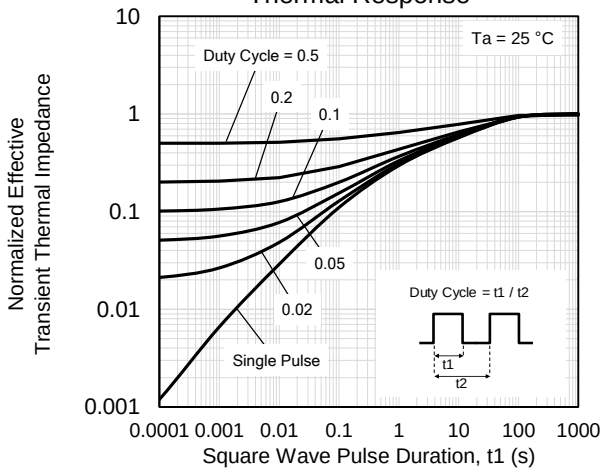
Rth - tsw



Safe Operating Area *2



Thermal Response *2



Note

*1 Pulse measurement.

*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad
(62 mm² area, 36 µm thickness).

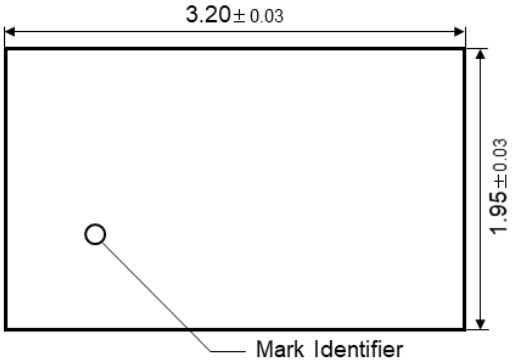
*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad
(612 mm² area, 36 µm thickness).

*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

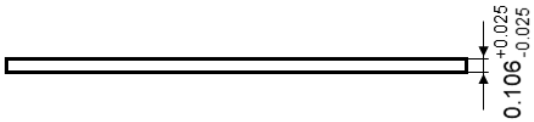
Package outline dimensions

(Top View)

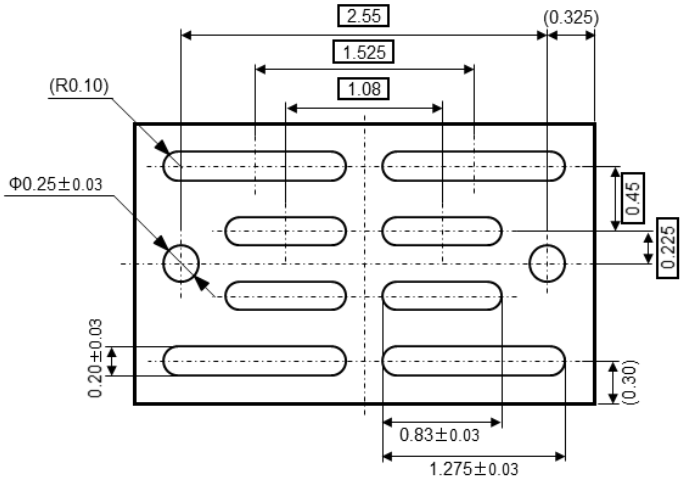
Unit: mm



(Front View)



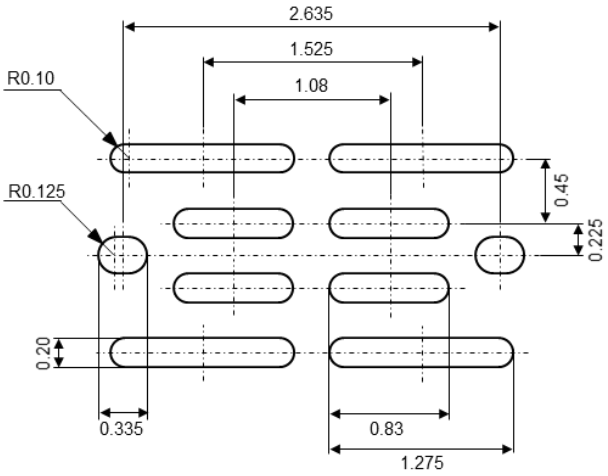
(Bottom View)



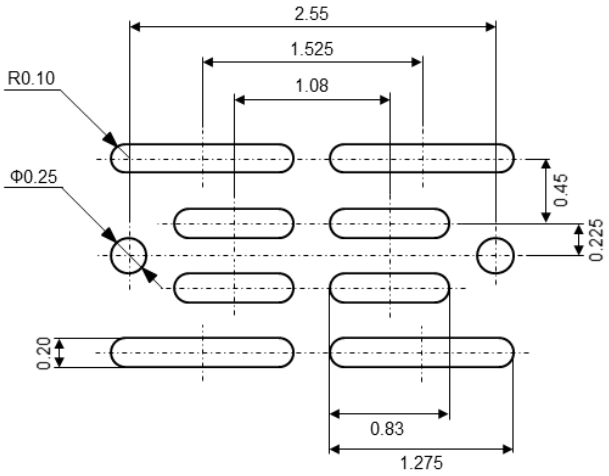
11. LAND & STENCIL PATTERN (Reference)

Unit: mm

LAND



STENCIL



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

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