

#### Product Summary

$V_{DS}$ (V)	$R_{DS(on),max}$ (mΩ)	$I_D$ (A)
-30	48 @ $V_{GS} = -10V$	-4.0

#### Features

- ❖ Fast Switching
- ❖ Low On-Resistance
- ❖ Low Gate Charge

#### Application

- ❖ Load Switch
- ❖ Motor Control
- ❖ Power Management

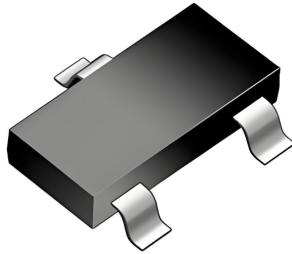
#### General Information

##### Shipping

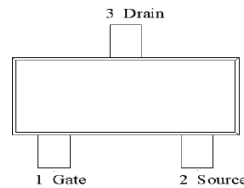
- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

##### Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

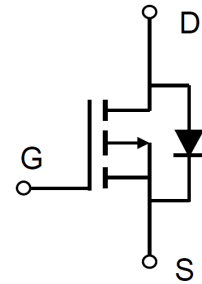


SOT-23



PIN Configuration  
(Top View)

#### Equivalent circuit



#### Absolute Maximum Rating ( $T_A=25^\circ\text{C}$ )

Parameter	Symbol	Limit	Unit
Drain-source voltage	$V_{DS}$	-30	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current ( $V_{GS}=-4.5V$ ) <sup>(1)</sup>	$I_D$	-4.0	A
		-3.2	
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	-16	
Power dissipation	$P_D$	1.1	W
		0.73	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter <sup>(4)</sup>						
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-30			V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.0	-1.5	-2.2	V
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
Drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.0 A		39	48	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.0 A		53	65	mΩ
Forward transconductance <sup>(5)</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -5.0V, I <sub>D</sub> = -4.0A		8.0		S
Gate resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1MHz		10		Ω
Dynamic <sup>(5)</sup>						
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4.0A V <sub>GS</sub> = -10V		12		nC
Gate-source charge	Q <sub>gs</sub>			1.5		
Gate-drain charge	Q <sub>gd</sub>			1.5		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -15V I <sub>D</sub> = -4.0A, R <sub>GEN</sub> = 3.0Ω		3.0		ns
Rise time	t <sub>r</sub>			7.7		
Turn-off delay time	t <sub>d(off)</sub>			23		
Fall time	t <sub>f</sub>			11		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		631		pF
Output capacitance	C <sub>oss</sub>			77		
Reverse transfer capacitance	C <sub>rss</sub>			62		
Reverse Diode Characteristics <sup>(5)</sup>						
Diode forward voltage	V <sub>SD</sub>	I <sub>S</sub> = -2.0A, V <sub>GS</sub> = 0V		-0.8	-1.2	V
Diode Forward Current	I <sub>s</sub>	T <sub>A</sub> = 25°C			-4.0	A

**Notes**

1. This current is chip limited, which is calculated based on  $R_{thjc}$ .
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Short duration pulse test used to minimize self-heating effect.
5. Defined by design, not subject to production.

**Thermal Characteristic (Ta=25°C)**

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient <sup>(3)</sup>	$R_{\theta JA}$	85	110	°C/W

## Electrical characteristics diagrams

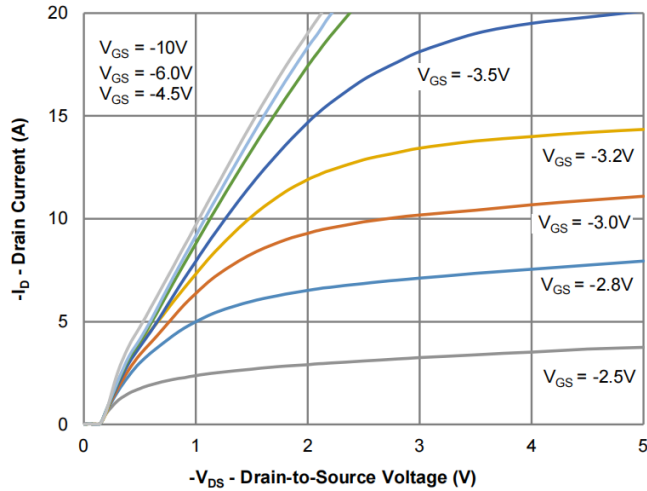


Figure 1: Output Characteristics

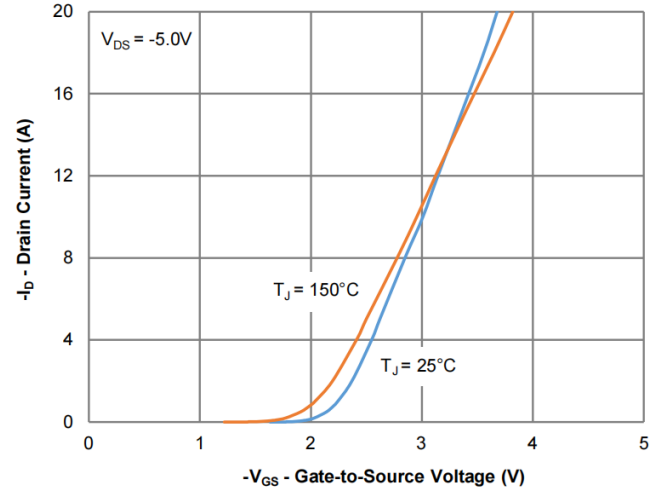


Figure 2: Transfer Characteristics

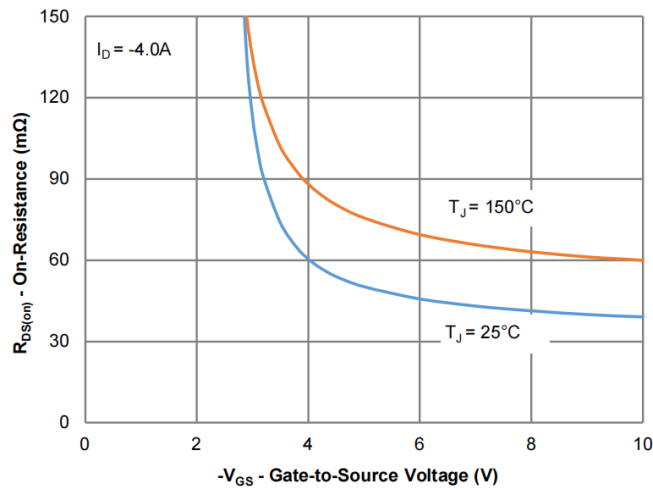


Figure 3: On-Resistance vs. Gate-Source Voltage

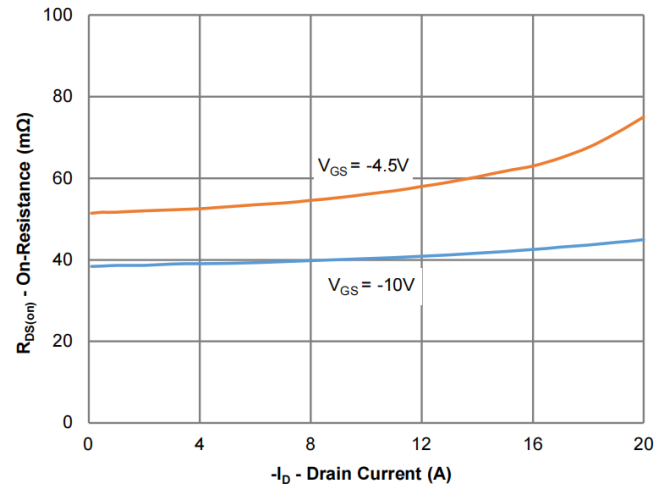


Figure 4: On-Resistance vs. Gate-Source Voltage

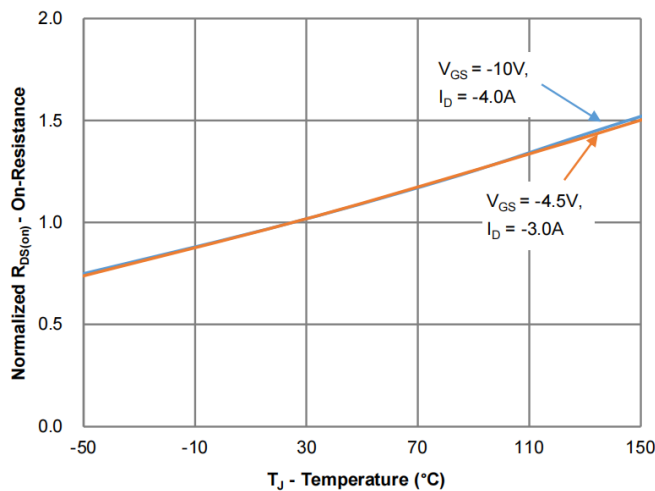


Figure 5: On-Resistance vs. Junction Temperature

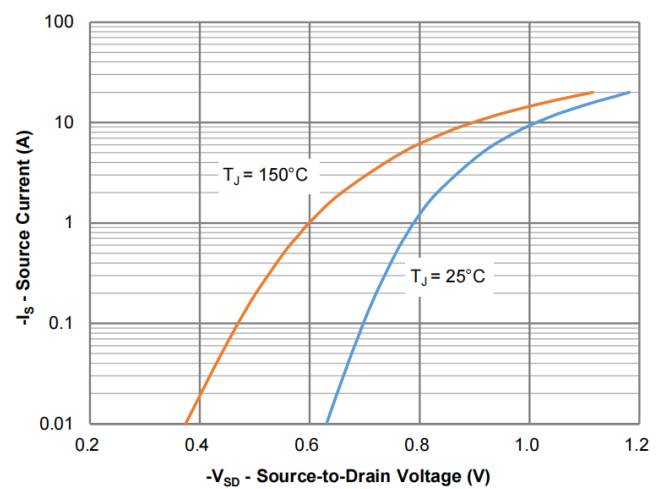


Figure 6: Source-Drain Diode Forward Voltage

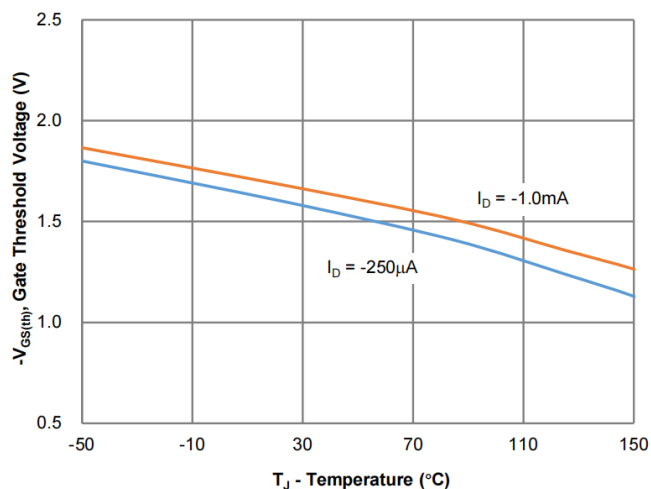


Figure 7: Gate Threshold Variation vs. Junction Temperature

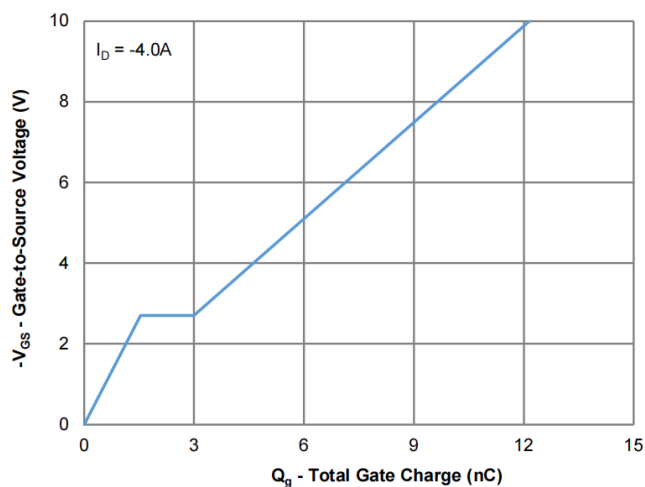


Figure 8: Gate Charge Characteristics

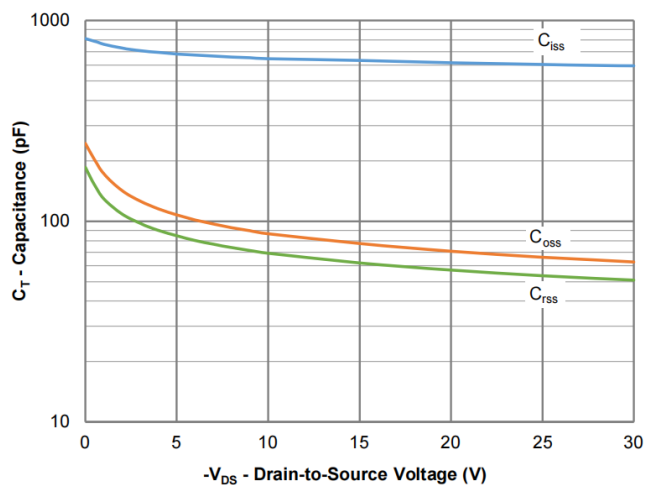


Figure 9: Capacitance Characteristics

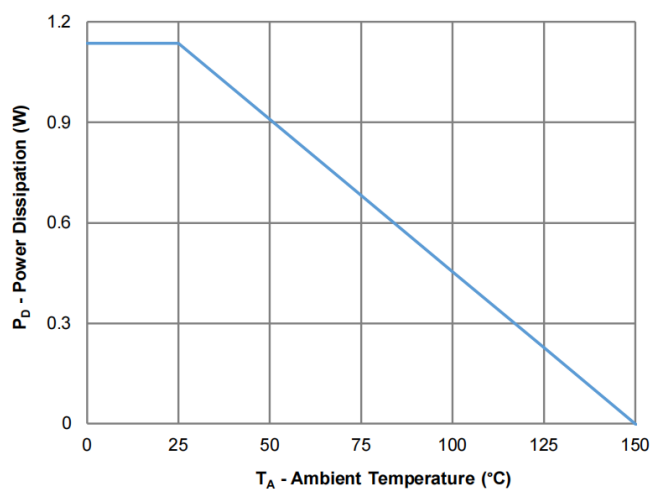


Figure 10: Power Derating

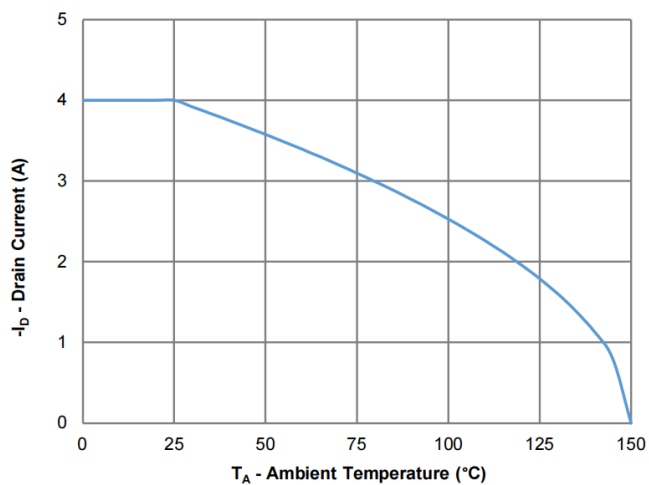


Figure 11: Current Derating

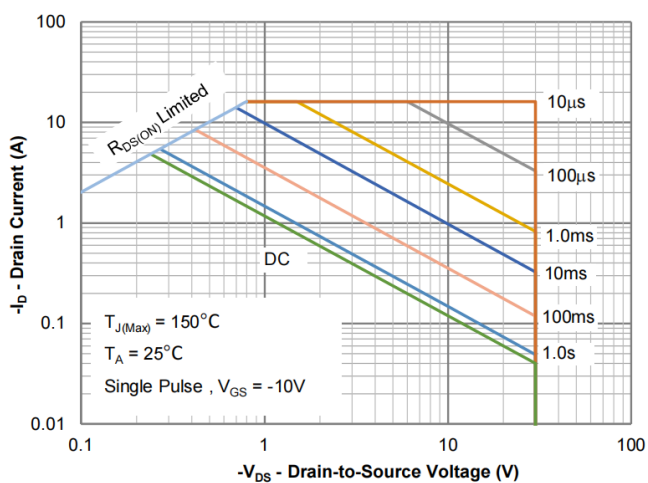


Figure 12: Safe Operating Area



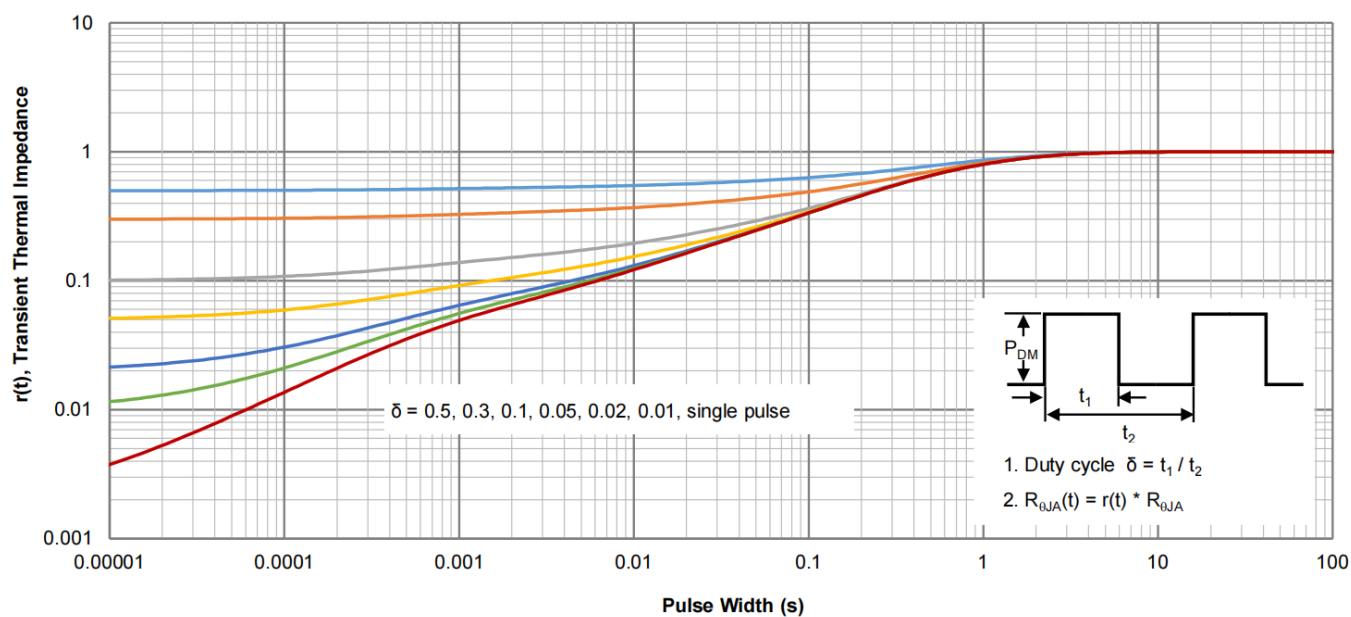
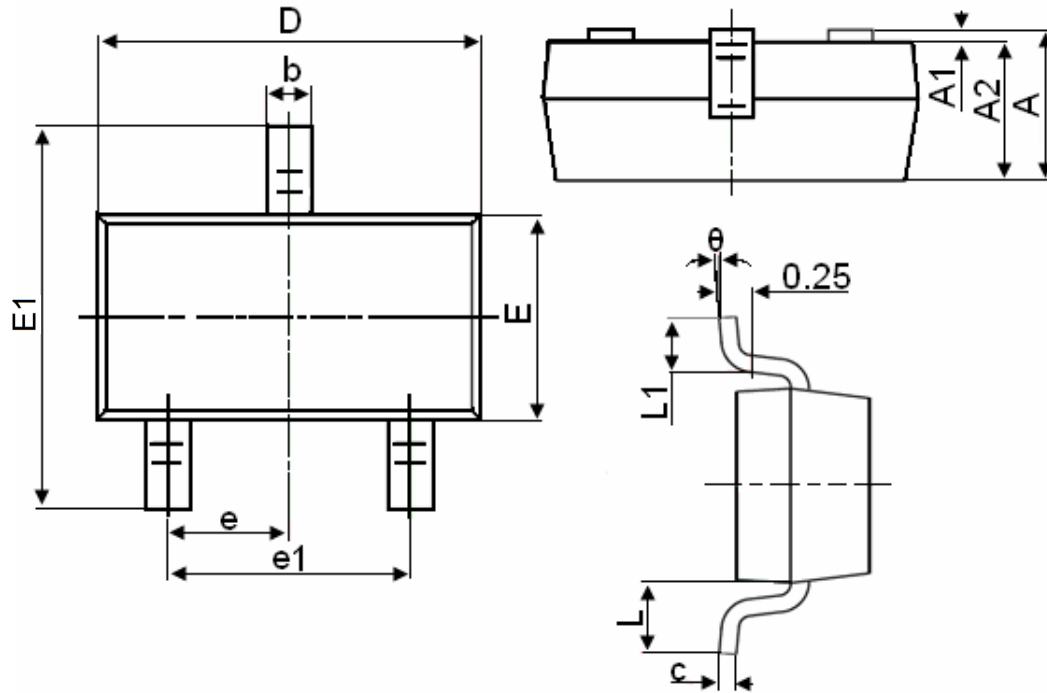


Figure 13: Normalized Maximum Transient Thermal Impedance

# Package outline dimensions SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.90	1.150
A1	0.0	0.100
A2	0.9	1.050
b	0.30	0.500
c	0.08	0.150
D	2.80	3.000
E	1.20	1.400
E1	2.2	2.550
e	0.950 TYP	
e1	1.8	2.000
L	0.55 REF	
L1	0.3	0.500
θ	0°	8°

## Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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