

Product Summary

| V_{DS} (V) | $R_{DS(on),max}$ (mΩ) | I_D (A) |
|--------------|-----------------------|-----------|
| -20 | 22 @ $V_{GS} = -4.5V$ | -7 |

Features

- ❖ Fast Switching
- ❖ Low On-Resistance
- ❖ Low Gate Charge

Application

- ❖ Load Switch
- ❖ Motor Control
- ❖ Power Management

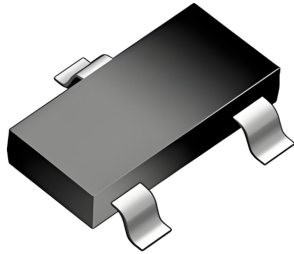
General Information

Shipping

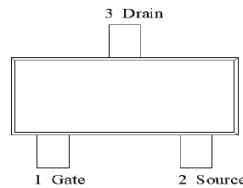
- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

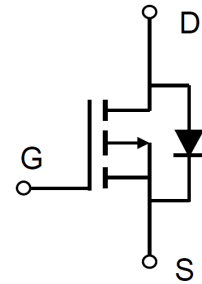


SOT23-3L



PIN Configuration
(Top View)

Equivalent circuit



Absolute Maximum Rating ($T_A=25^\circ\text{C}$)

| Parameter | Symbol | Limit | Unit |
|--|----------------|------------|------------------|
| Drain-source voltage | V_{DS} | -20 | V |
| Gate-source voltage | V_{GS} | ± 12 | |
| Continuous drain current ($V_{GS}=-4.5V$) ⁽¹⁾ | I_D | -7 | A |
| | | -5.4 | |
| Pulsed drain current ⁽²⁾ | $I_{D,pulse}$ | -30 | |
| Power dissipation | P_D | 1.31 | W |
| | | 0.74 | W |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to 150 | $^\circ\text{C}$ |

Thermal Characteristic ($T_A=25^\circ\text{C}$)

| Parameter | Symbol | Typ. | Max. | Unit |
|--|-----------------|------|------|--------------------|
| Thermal Resistance, Junction-to-Ambient ⁽³⁾ | $R_{\theta JA}$ | 125 | --- | $^\circ\text{C/W}$ |
| Thermal Resistance, Junction-to-case ⁽³⁾ | $R_{\theta JC}$ | 7.4 | --- | $^\circ\text{C/W}$ |

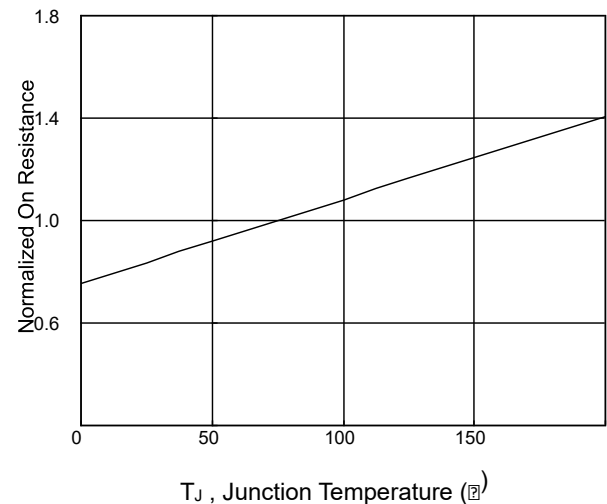
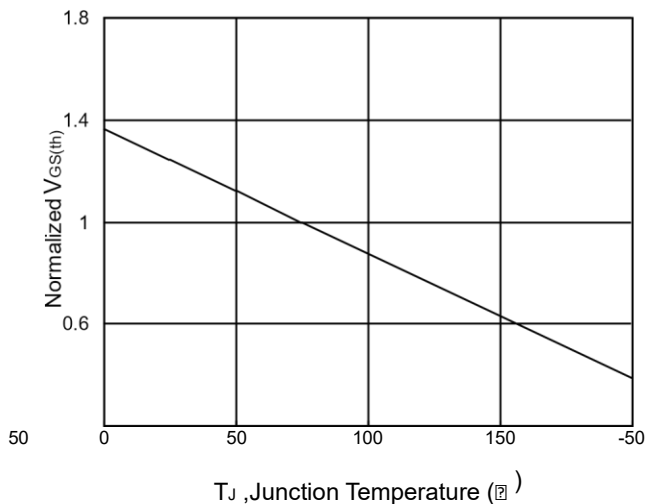
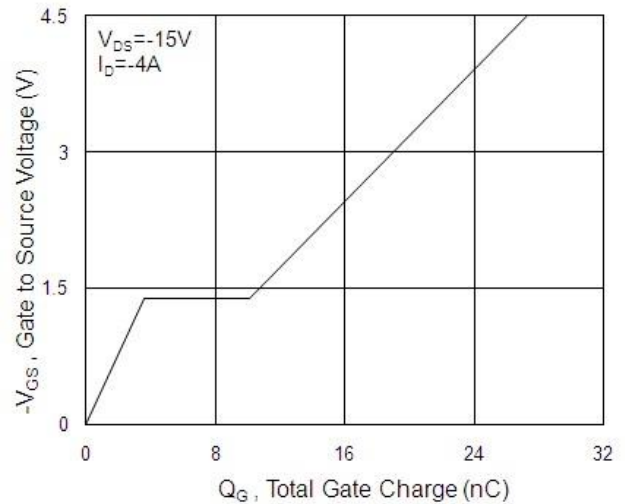
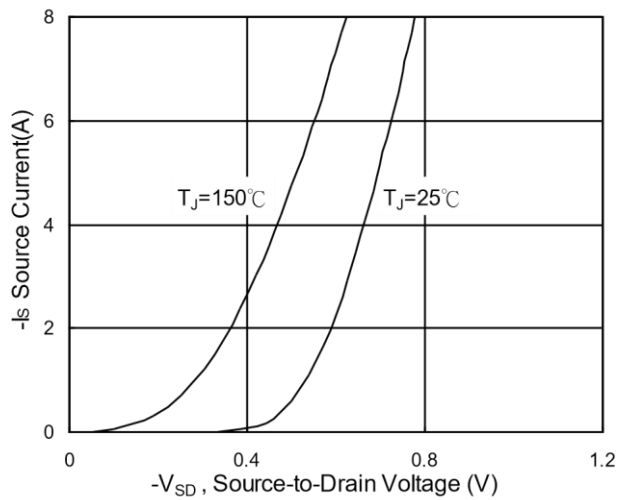
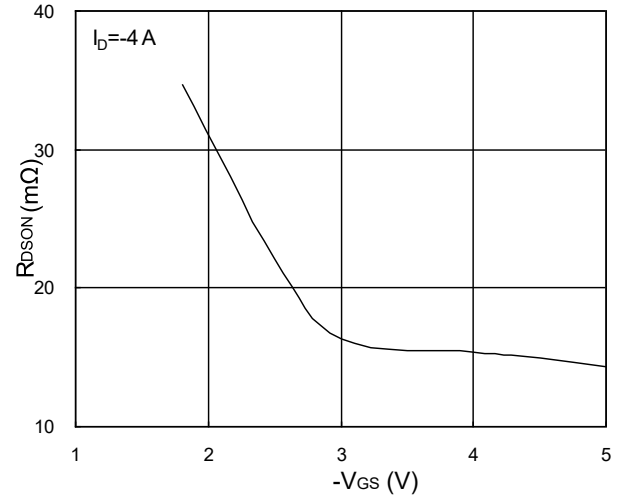
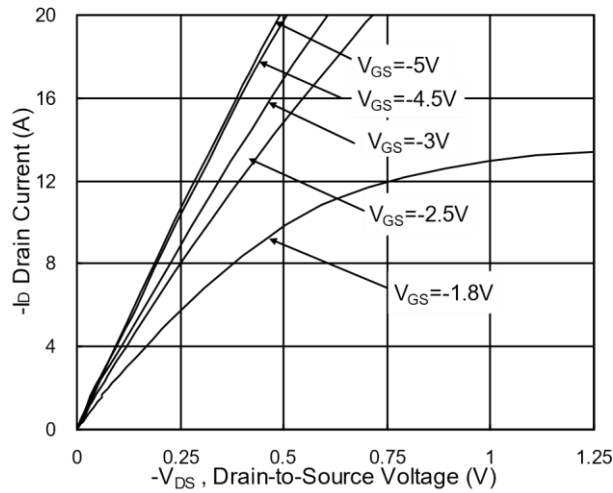
**Electrical characteristics (Ta=25°C ± 3°C)**

| Parameter | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|--|----------------------|---|-------|-------|------|------|
| Static parameter ⁽⁴⁾ | | | | | | |
| Drain to source breakdown voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = -250 μA | -20 | | | V |
| Gate-source threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = -250 μA | -0.45 | -0.65 | -0.9 | V |
| Gate-body leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±12 V | | | ±100 | nA |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = -20 V, V _{GS} = 0 V | | | -1 | μA |
| Drain-source on-resistance | R _{DS(on)} | V _{GS} = -4.5V, I _D = -4.1 A | | 18.9 | 22 | mΩ |
| | | V _{GS} = -2.5V, I _D = -2.5 A | | 23.1 | 25.1 | mΩ |
| Forward transconductance | g _{fs} | V _{DS} = -5.0V, I _D = -3A | | 12.8 | | S |
| Gate resistance | R _g | V _{GS} = 0V, V _{DS} = 0V, f = 1MHz | | 21 | | Ω |
| Dynamic ⁽⁵⁾ | | | | | | |
| Total gate charge | Q _g | V _{DS} = -15V, I _D = -3A V _{GS} = -4.5V | | 10.2 | | nC |
| Gate-source charge | Q _{gs} | | | 1.89 | | |
| Gate-drain charge | Q _{gd} | | | 3.1 | | |
| Turn-on delay time | t _{d(on)} | V _{GS} = -4.5V, V _{DS} = -10V I _D = -3A, R _{GEN} = 3.3 | | 5.6 | | ns |
| Rise time | t _r | | | 40.8 | | |
| Turn-off delay time | t _{d(off)} | | | 33.6 | | |
| Fall time | t _f | | | 18 | | |
| Input capacitance | C _{iss} | V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz | | 857 | | pF |
| Output capacitance | C _{oss} | | | 114 | | |
| Reverse transfer capacitance | C _{rss} | | | 108 | | |
| Reverse Diode Characteristics ⁽⁵⁾ | | | | | | |
| Diode forward voltage | V _{SD} | I _S = -2.0A, V _{GS} = 0V | | -0.8 | -1.2 | V |
| Diode Forward Current | I _s | T _A = 25°C | | | -7 | A |
| Reverse Recovery Time | V _{SD} | I _F = -3.0A, di/dt=100A/μs, T _J = 25°C | | 21.8 | | nS |
| Reverse Recovery Charge | I _s | | | 6.9 | | nC |

Notes

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Short duration pulse test used to minimize self-heating effect.
5. Defined by design, not subject to production.

Electrical characteristics diagrams



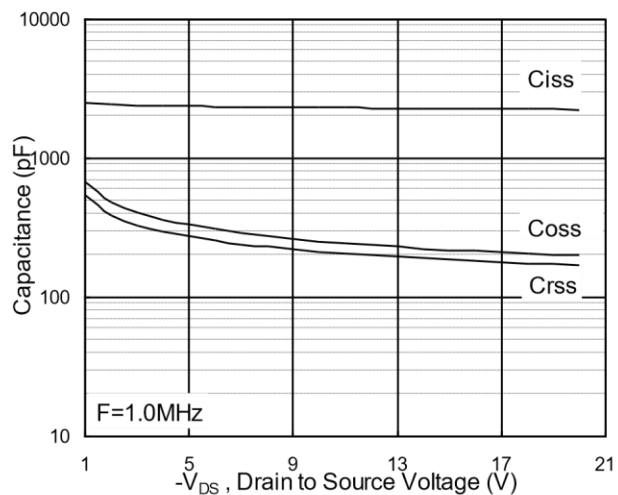


Fig.7 Capacitance

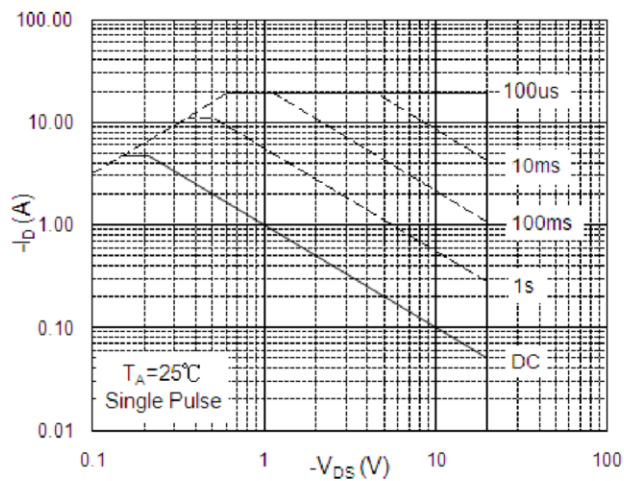


Fig.8 Safe Operating Area

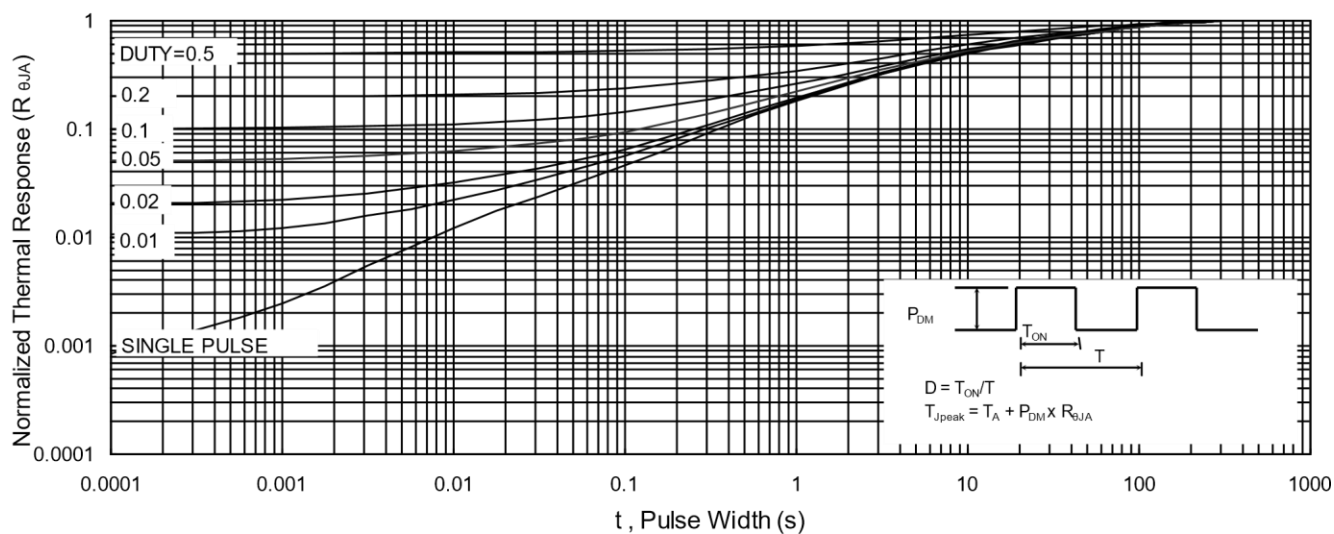
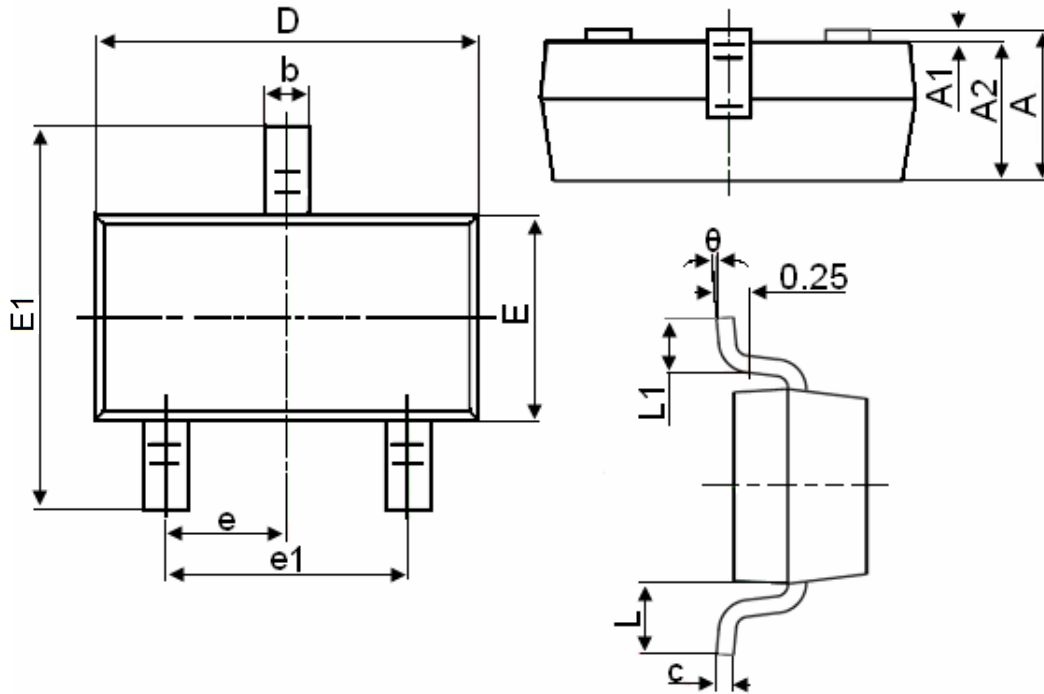


Fig.9 Normalized Maximum Transient Thermal Impedance

Package outline dimensions SOT23-3L



| Symbol | Dimensions in Millimeters | |
|----------|---------------------------|-------|
| | MIN. | MAX. |
| A | 0.90 | 1.150 |
| A1 | 0.0 | 0.100 |
| A2 | 0.9 | 1.050 |
| b | 0.30 | 0.500 |
| c | 0.08 | 0.150 |
| D | 2.80 | 3.000 |
| E | 1.50 | 1.700 |
| E1 | 2.65 | 2.950 |
| e | 0.950 TYP | |
| e1 | 1.8 | 2.000 |
| L | 0.55 REF | |
| L1 | 0.3 | 0.500 |
| θ | 0° | 8° |

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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