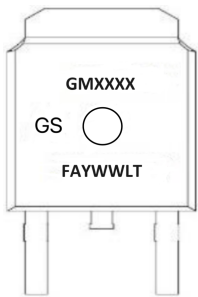
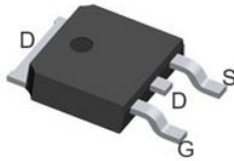


Product Summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
60	5.5 @ $V_{GS} = 10V$	80

View and Internal Schematic Diagram



TO-252

NOTE:
 LOGO - GS
 GMXXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

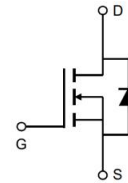
Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Application

- Primary side switch
- Synchronous rectification
- DC/DC conversion
- Load switching
- Boost converters
- DC/AC inverters

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	60	V
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C ⁽¹⁾	I _D	80	A
	T _C =100°C		50	
Pulsed drain current ⁽²⁾		I _{D,pulse}	240	
Avalanche energy, single pulse ⁽³⁾		E _{AS}	132	mJ
Power dissipation	T _C =25°C	P _D	78	W
	T _C =100°C		31	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to 150	°C

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	1.6	$^\circ\text{C/W}$
Thermal resistance, junction-to-ambient ⁽⁴⁾	$R_{\theta JA}$	50	

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	60			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 100 A		5.0	5.5	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 100 A		121		S
Gate resistance	R _g	f = 1 MHz		1.0		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 30 V, I _D = 20 A, V _{GS} = 10 V		31		nC
Gate-source charge	Q _{gs}			6		
Gate-drain charge	Q _{gd}			5		
Turn-on delay time	t _{d(on)}	V _{DS} = 30 V, I _D = 20 A, V _{GS} = 10 V, R _{GEN} = 3 Ω		10		ns
Rise time	t _r			34		
Turn-off delay time	t _{d(off)}			26		
Fall time	t _f			45		
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		3712		pF
Output capacitance	C _{oss}			296		
Reverse transfer capacitance	C _{rss}			251		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 100 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 30 V, I _F = 50 A, di/dt = 100 A/μs		79		ns
Reverse recovery charge	Q _{rr}			180		nC

Notes

- (1) Limited by maximum junction temperature..
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 30\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 0.5\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

Typical Performance Characteristics

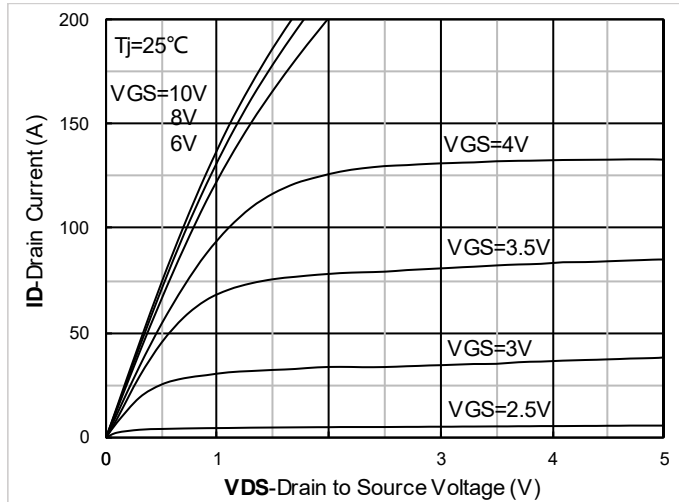


Figure 1. Output Characteristics

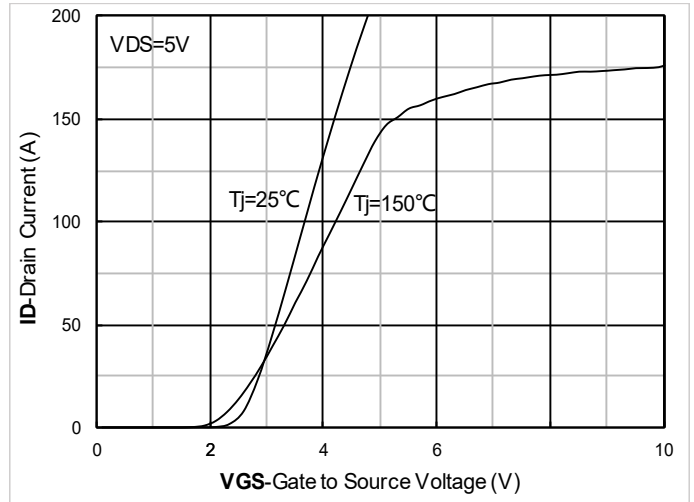


Figure 2. Transfer Characteristics

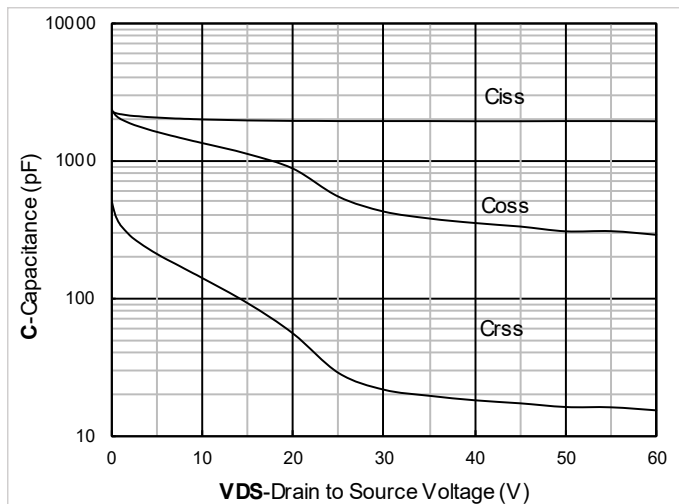


Figure 3. Capacitance Characteristics

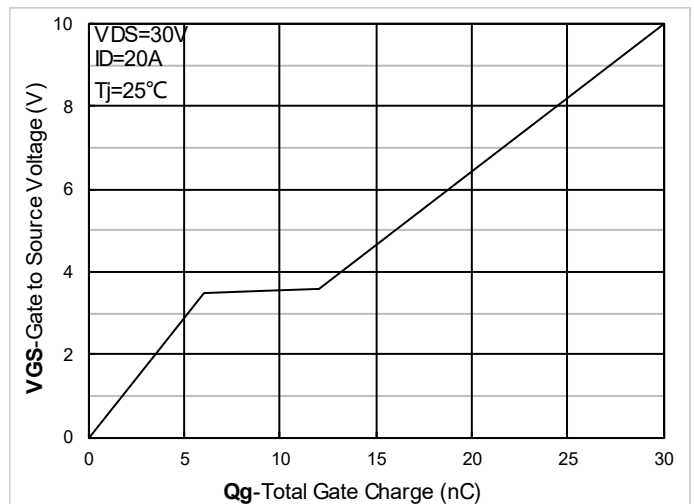


Figure 4. Gate Charge

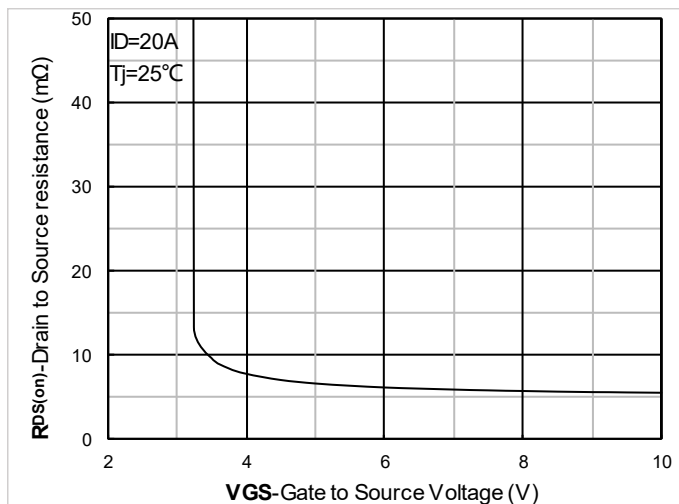


Figure 5. On-Resistance vs Gate to Source Voltage

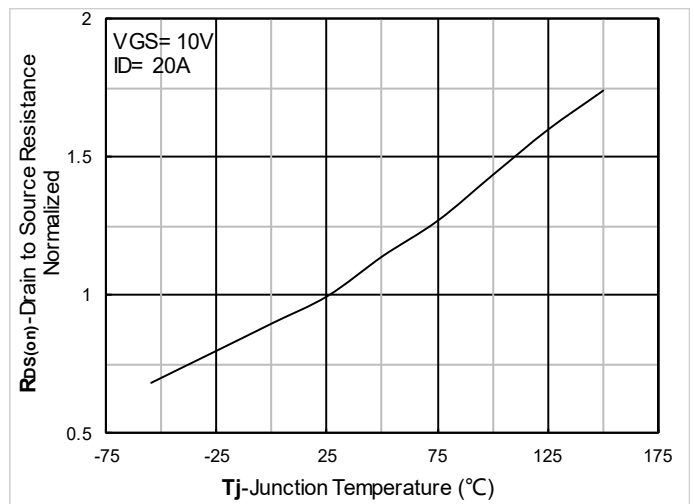


Figure 6. Normalized On-Resistance

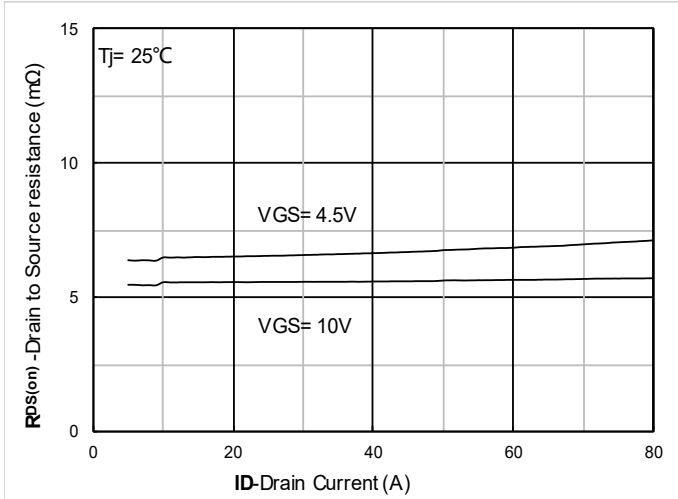


Figure 7. $R_{DS(on)}$ VS Drain Current

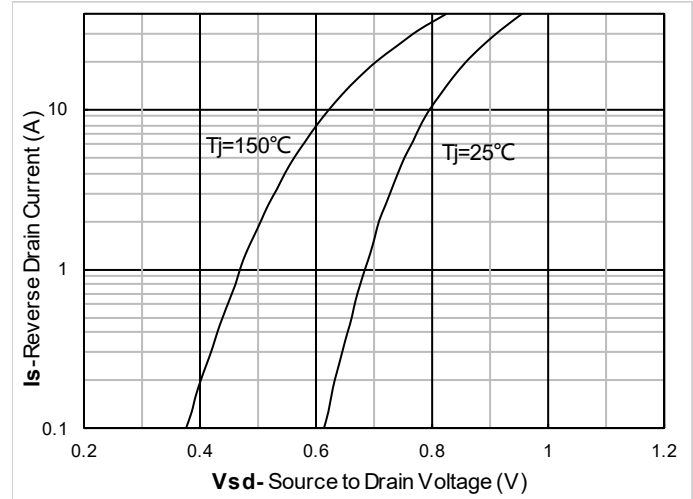


Figure 8. Forward characteristics of reverse diode

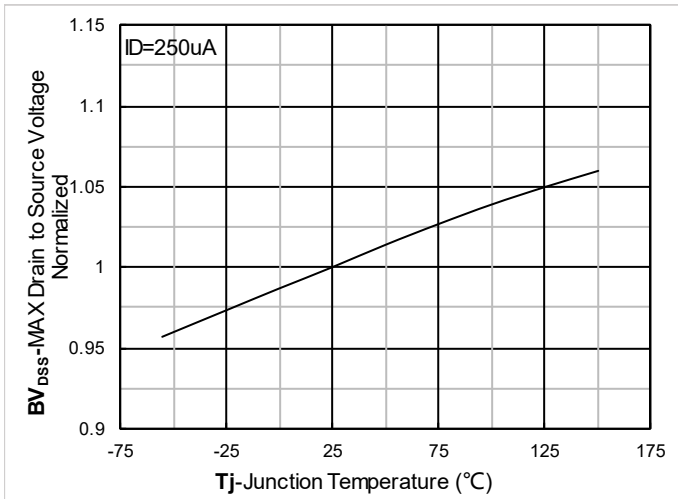


Figure 9. Normalized breakdown voltage

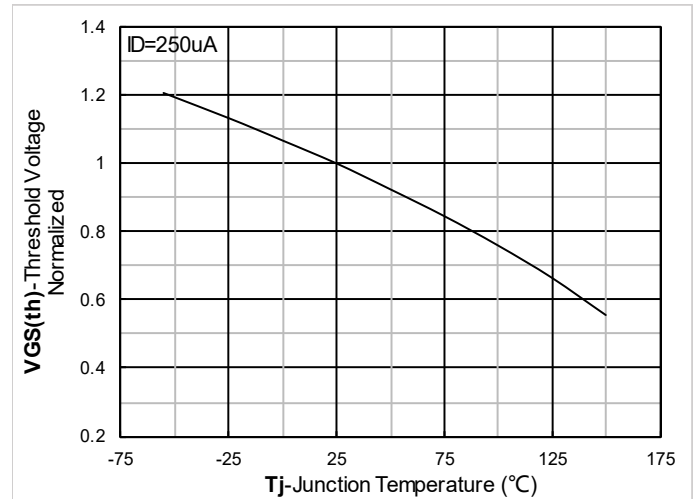


Figure 10. Normalized Threshold voltage

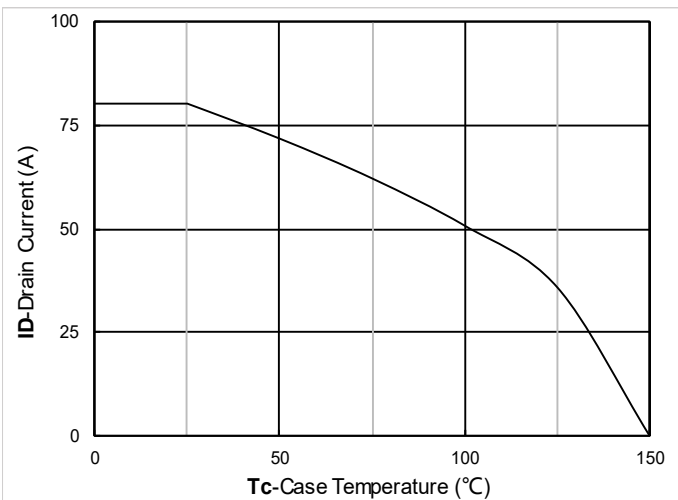


Figure 11. Current dissipation

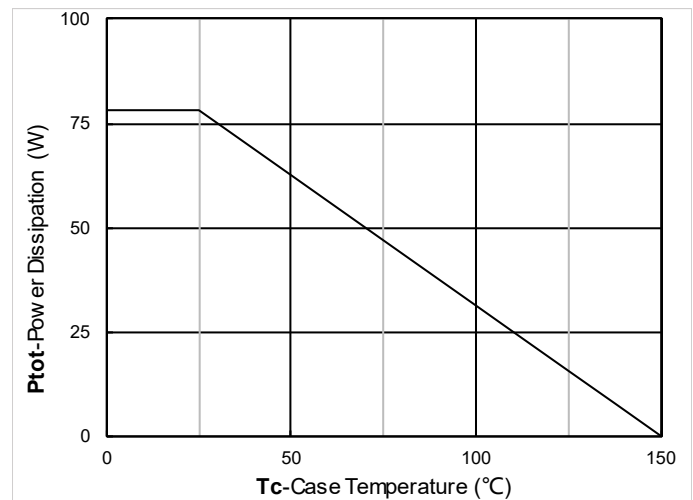


Figure 12. Power dissipation

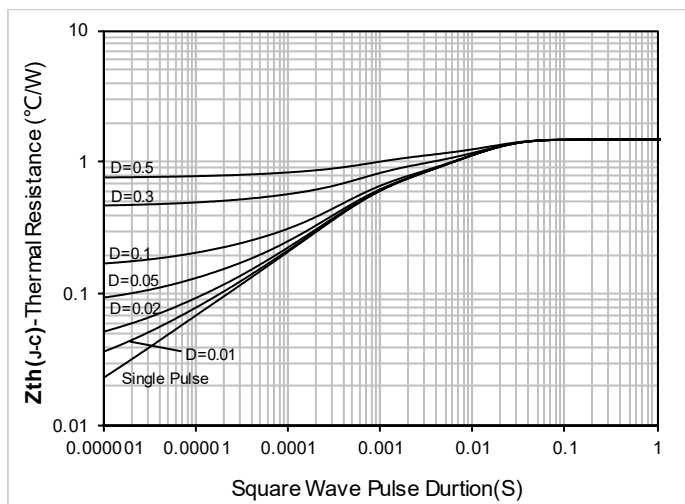


Figure 13. Maximum Transient Thermal Impedance

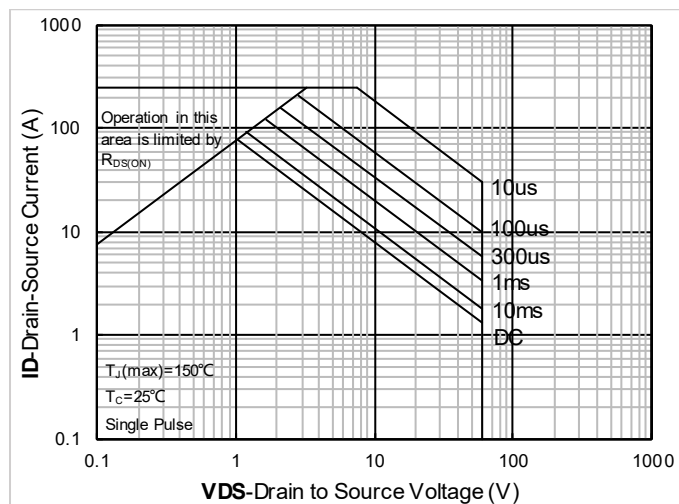


Figure 14. Safe Operation Area

Test Circuits & Waveforms

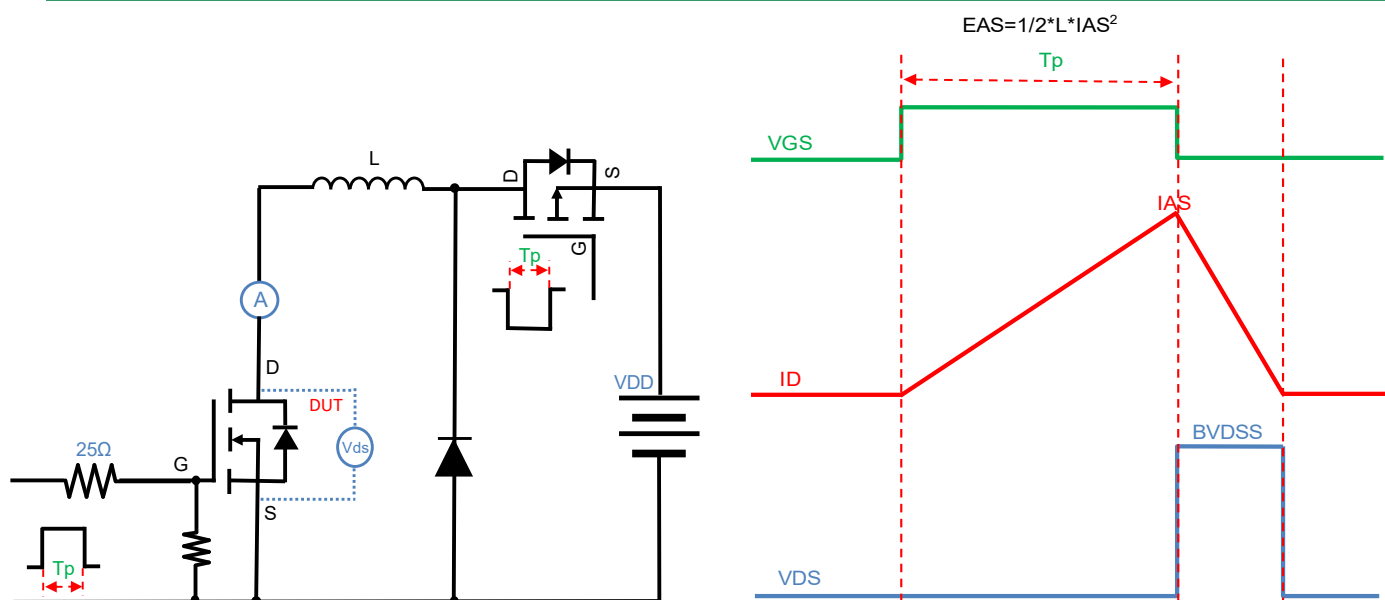


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

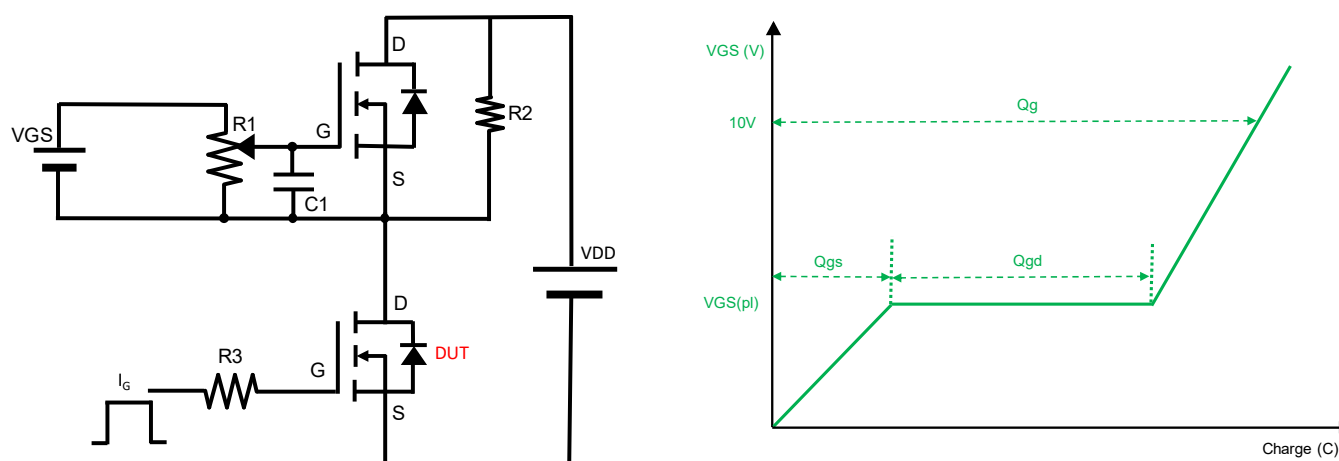


Figure B. Gate Charge Test Circuit & Waveform

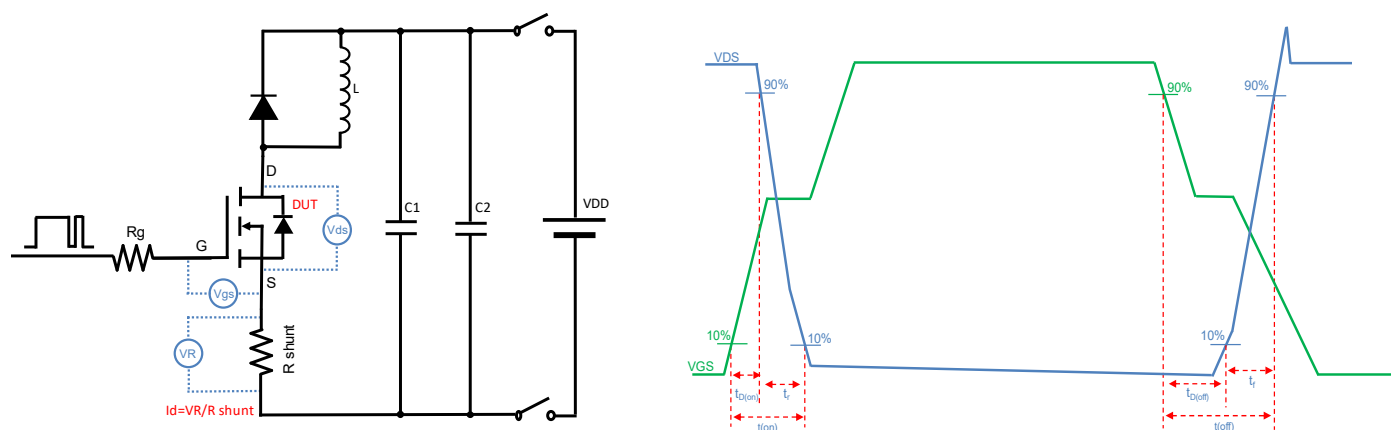


Figure C. Resistive Switching Test Circuit & Waveform

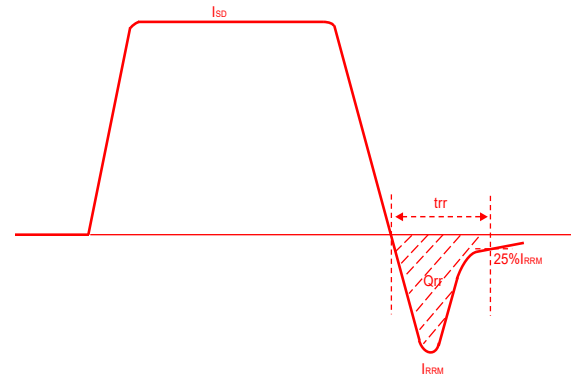
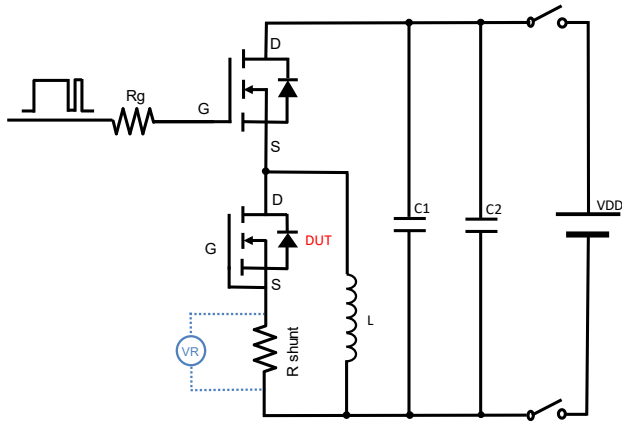
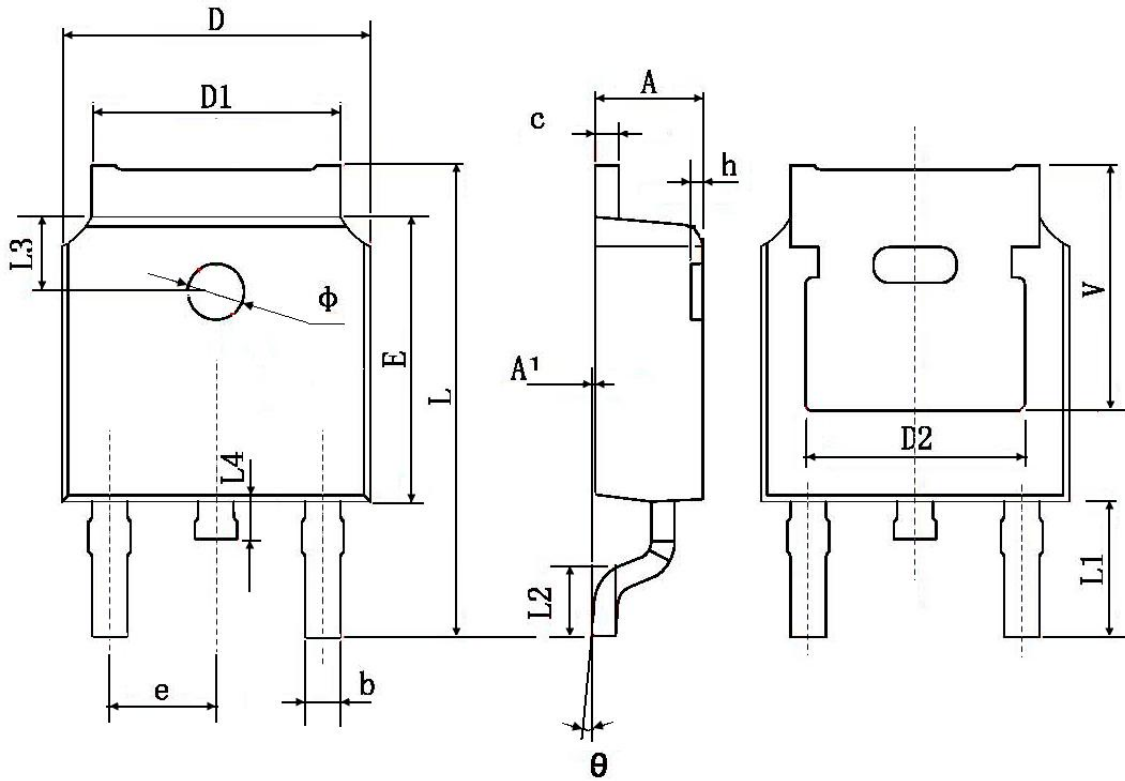


Figure D. Diode Recovery Test Circuit & Waveform

Package outline dimensions: TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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