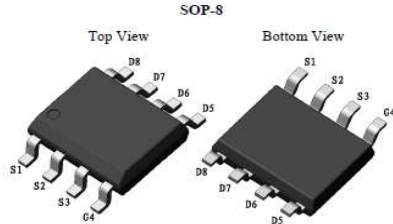


Product Summary

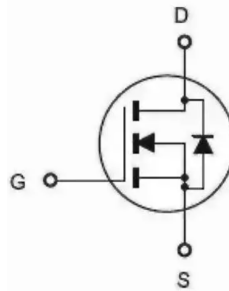
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
150	60 @ $V_{GS} = 10V$	20.2

View and Internal Schematic Diagram



NOTE:
 LOGO - GS
 GMS600N15B Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

Equivalent circuit



Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Application

- Primary side switch
- Synchronous rectification
- DC/DC conversion
- Load switching
- Boost converters
- DC/AC inverters

Absolute maximum rating@25°C

PARAMETER		SYMBOL	LIM	UNIT
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	$T_C = 25\text{ °C}$	I_D	20.2	A
	$T_C = 70\text{ °C}$		16	
Pulsed Drain Current ($t = 300\text{ μs}$)		I_{DM}	50	A
Single Pulse Avalanche Energy	$L = 0.1\text{ mH}$	E_{AS}	5	mJ
Maximum Power Dissipation	$T_C = 25\text{ °C}$	P_D	52	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c,d}			260	

Thermal Characteristic

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient	$t \leq 10\text{ s}$	R_{thJA}	26	33	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	1.9	2.4	

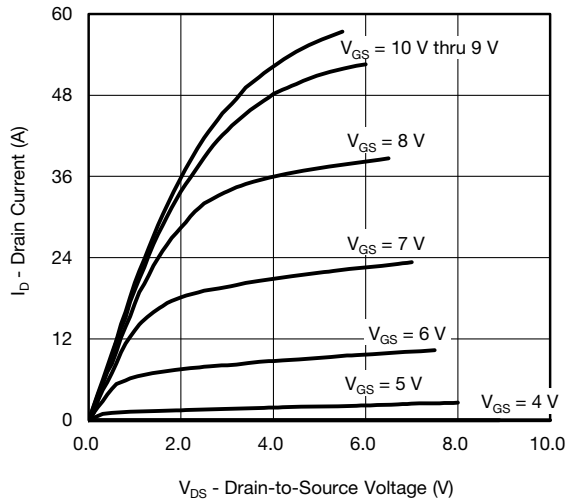
Electrical Characteristics (T_J=25 °C unless otherwise noted)

PARAMETER	S MBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	150			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		97		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			-6.9			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3	3.3	4.2	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 150 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 150 V, V _{GS} = 0 V, T _J = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		57	60	mΩ	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A		11		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz		420		pF	
Output Capacitance	C _{oss}			130			
Reverse Transfer Capacitance	C _{rss}			16			
Total Gate Charge	Q _g	V _{DS} = 75 V, V _{GS} = 10 V, I _D = 10 A		9.5	14.5	nC	
Gate-Source Charge	Q _{gs}	V _{DS} = 75 V, V _{GS} = 7.5 V, I _D = 10 A		7.6	11.5		
Gate-Drain Charge	Q _{gd}			2.5			
Output Charge	Q _{oss}			3.6			
Gate Resistance	R _g	V _{DS} = 75 V, V _{GS} = 0 V		23.6	36		
Turn-On Delay Time	t _{d(on)}	f = 1 MHz V _{DD} = 75 V, R _L = 7.5 Ω I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω		1.3		Ω	
Rise Time	t _r			13	26		
Turn-Off Delay Time	t _{d(off)}			11	22		
Fall Time	t _f			14	28		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 75 V, R _L = 7.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		9	18		ns
Rise Time	t _r			12	24		
Turn-Off Delay Time	t _{d(off)}			8	6		
Fall Time	t _f			13	26		
				8	16		
Drain-Source Body Diode Characteristics							
Body Diode Voltage	V _{SD}	I _S = 4 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		94	180	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			190	380	nC	
Reverse Recovery Fall Time	t _a			35		ns	
Reverse Recovery Rise Time	t _b			59			

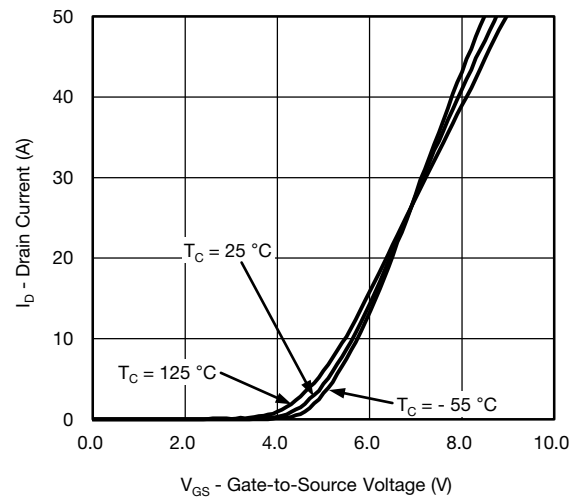
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

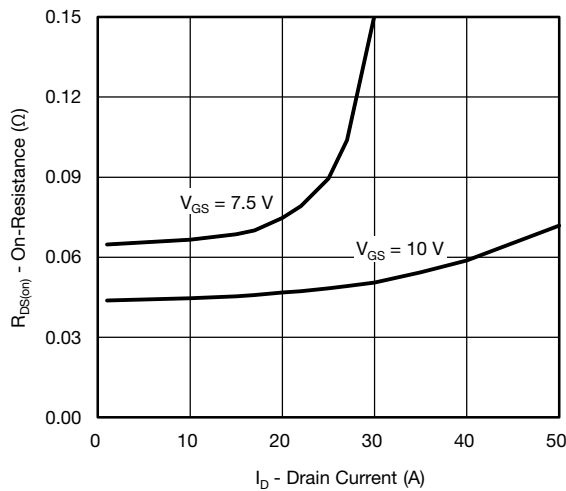
Typical Performance Characteristics



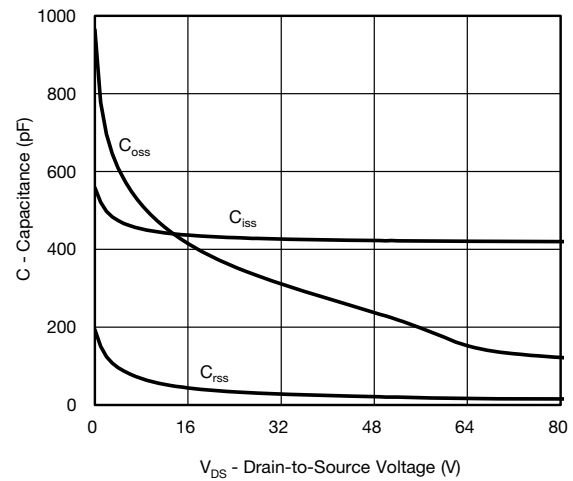
Output Characteristics



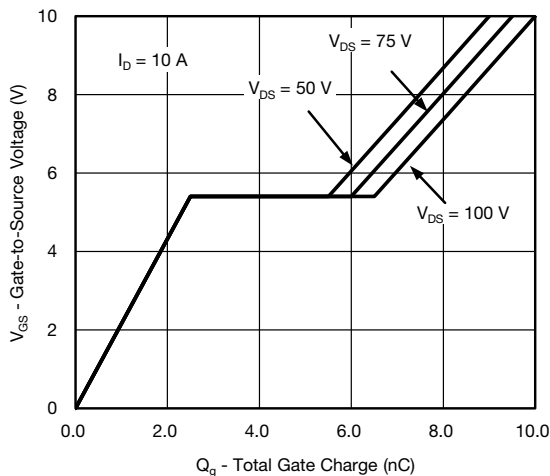
Transfer Characteristics



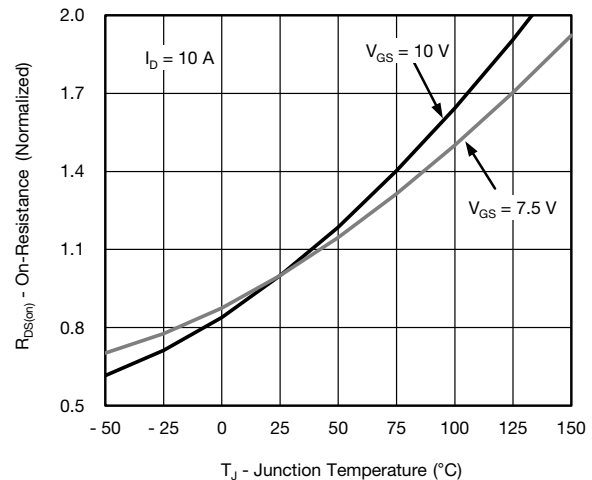
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

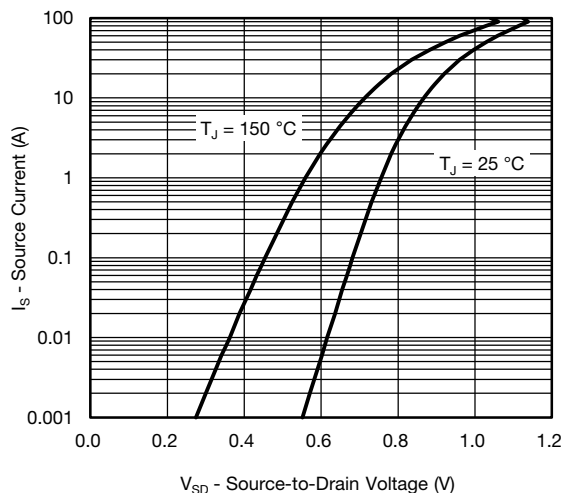


Gate Charge

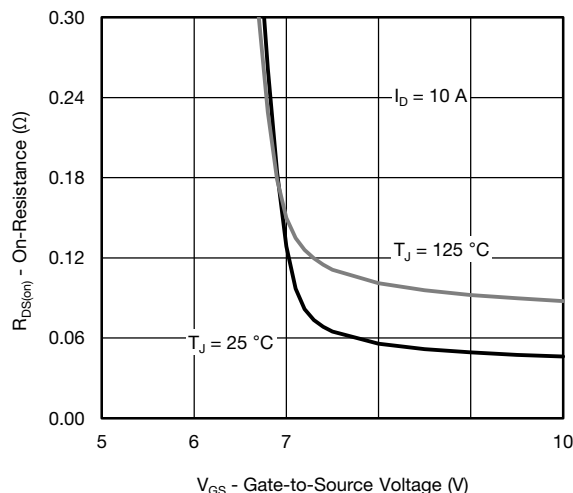


On-Resistance vs. Junction Temperature

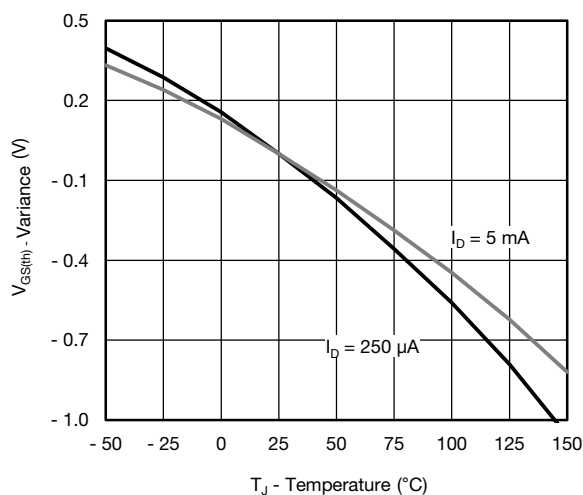
Typical Performance Characteristics



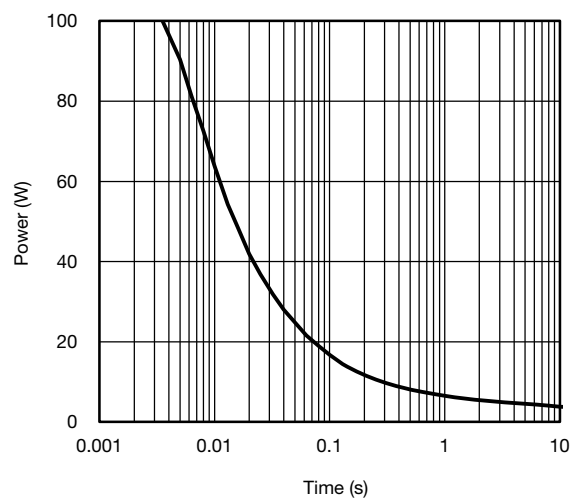
Source-Drain Diode Forward Voltage



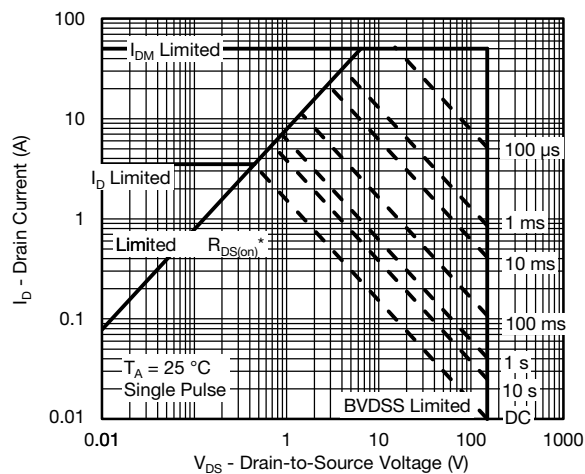
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

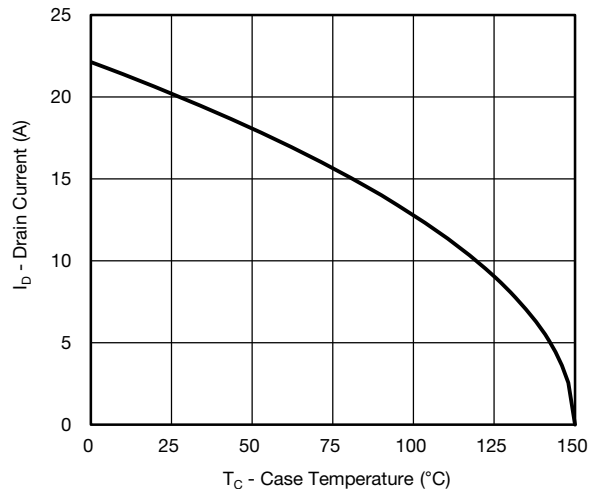


Single Pulse Power, Junction-to-Ambient

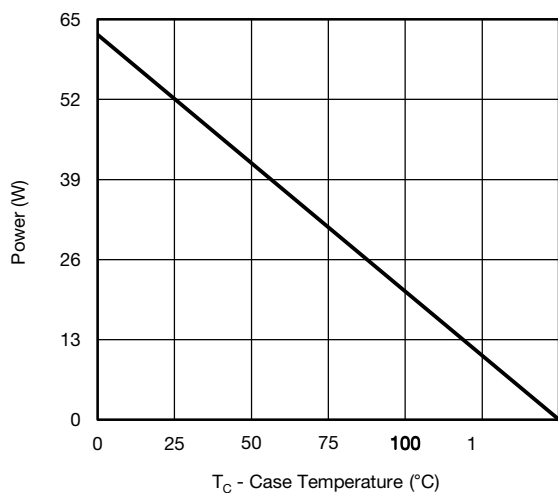


Safe Operating Area, Junction-to-Ambient

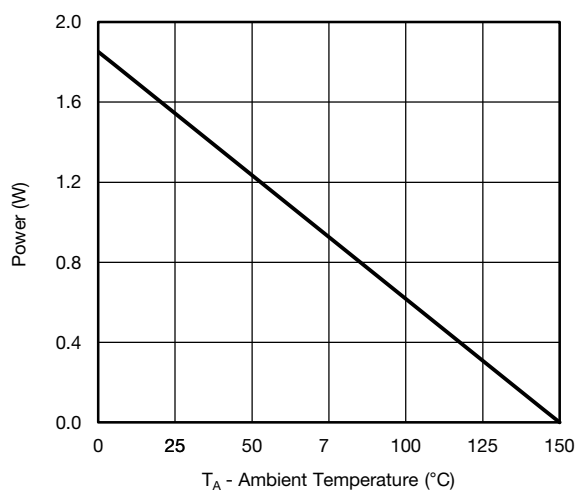
Typical Performance Characteristics



Current Derating*



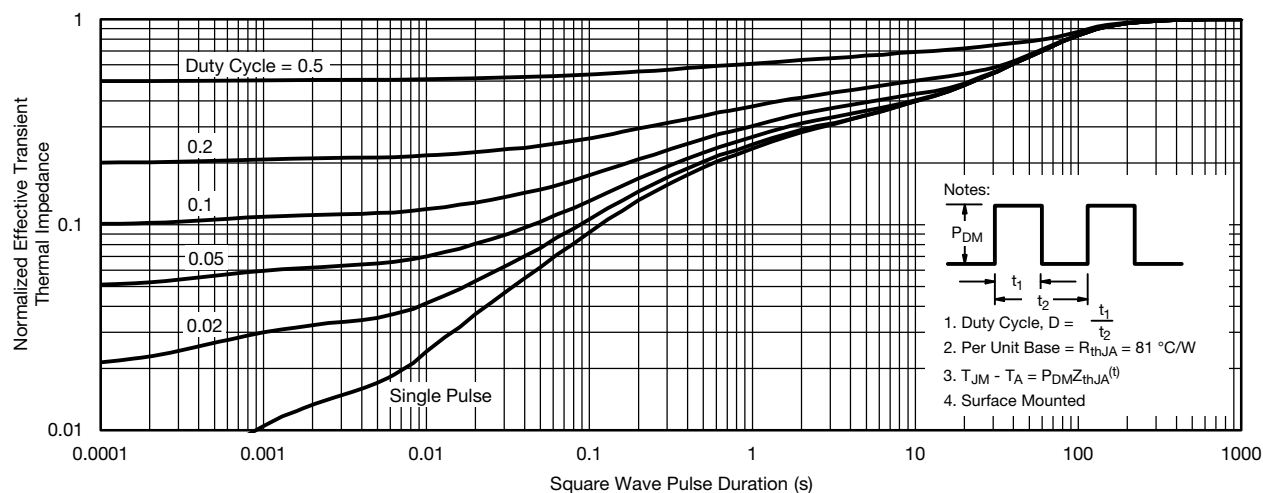
Power, Junction-to-Case



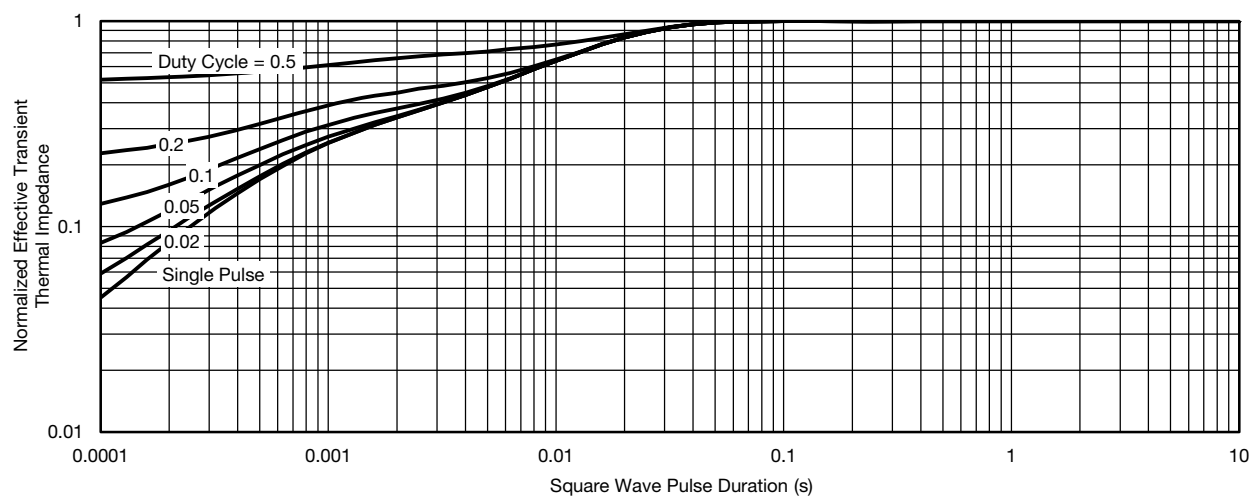
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Typical Performance Characteristics



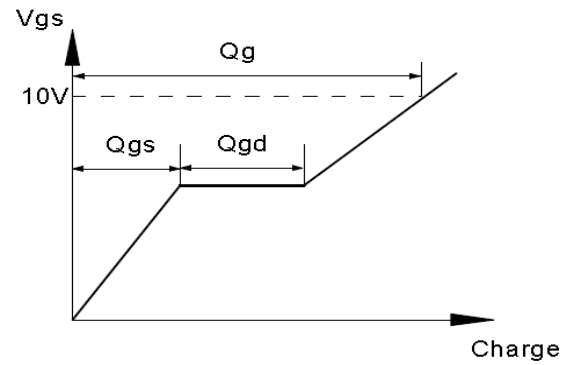
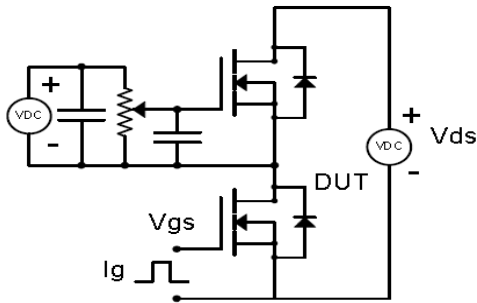
Normalized Thermal Transient Impedance, Junction-to-Ambient



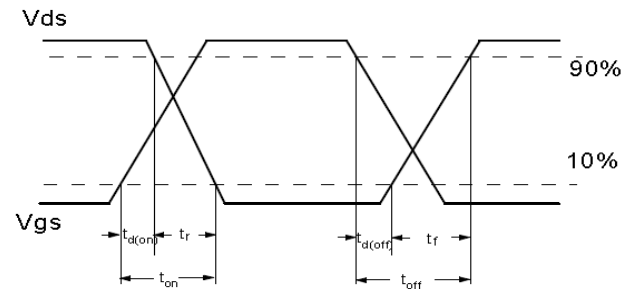
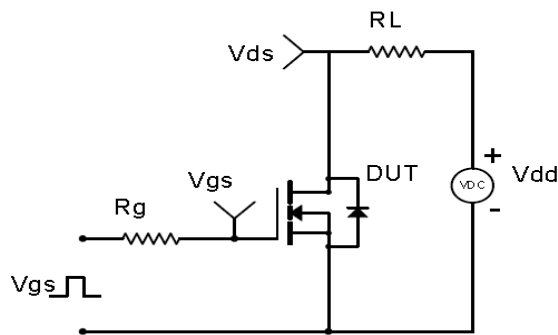
Normalized Thermal Transient Impedance, Junction-to-Case

Test Circuit & Waveform

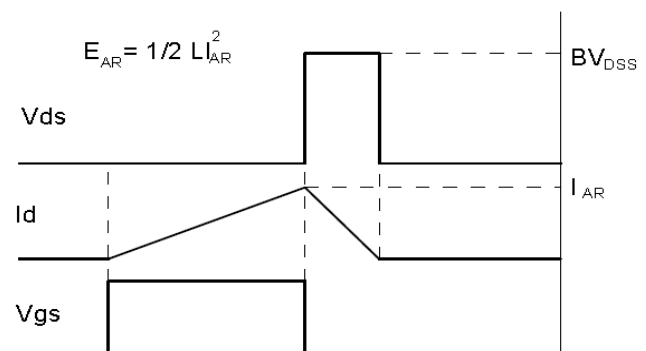
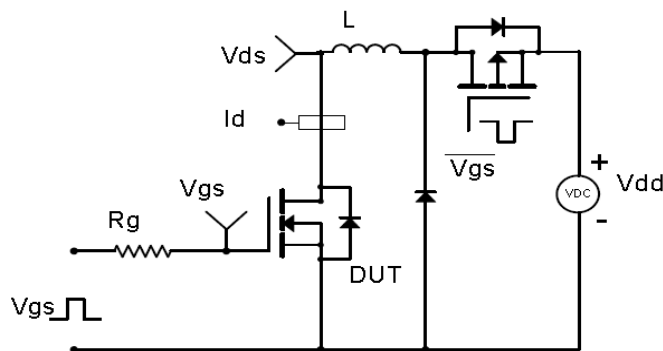
Gate Charge Test Circuit & Waveform



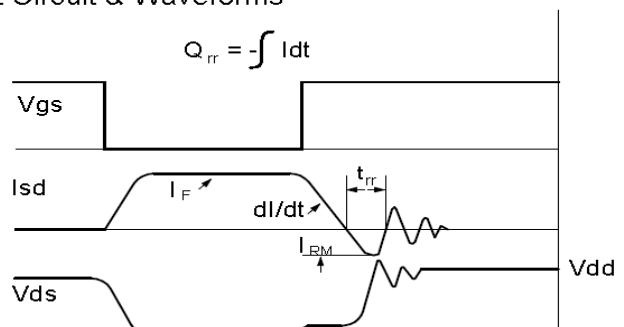
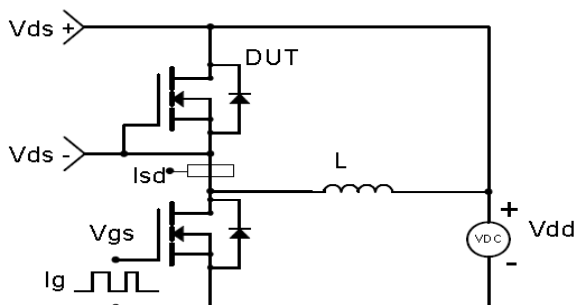
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

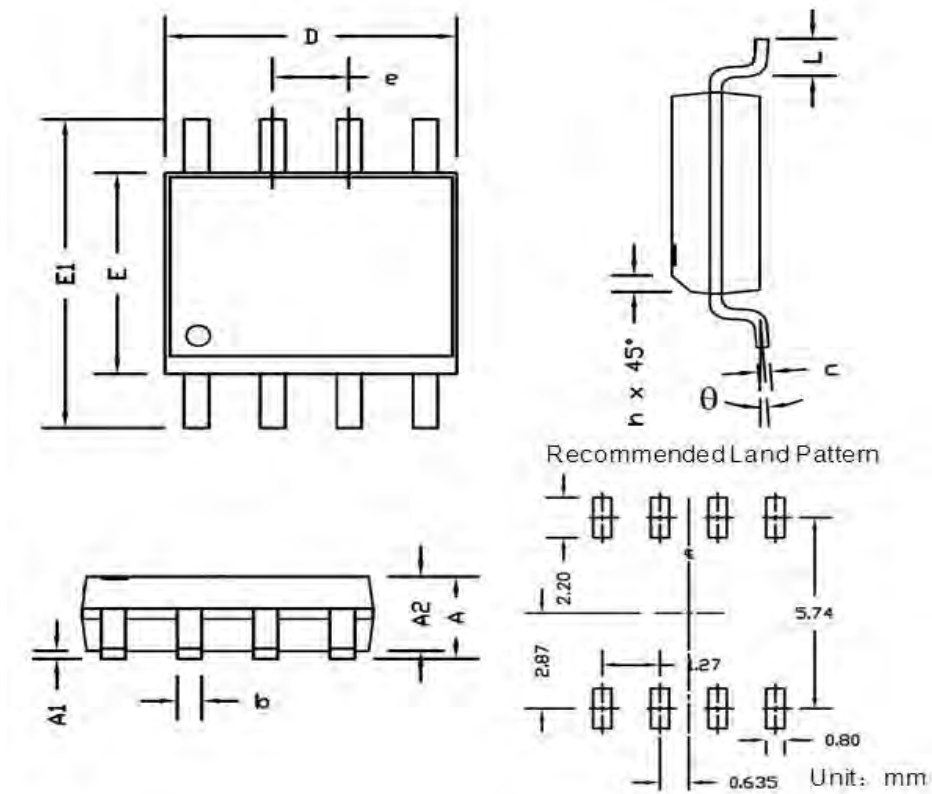


Diode Recovery Test Circuit & Waveforms



Outline Drawing SOP-8

Package Outline: SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
b	0.33	0.51	0.013	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
e	1.27 BSC.		0.050 BSC.	
E	3.80	4.00	0.150	0.157
E1	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

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