

Product Summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
200	22 @ $V_{GS} = 10V$	61 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Application

- DC/DC conversion
- Power switch
- Synchronous Rectification in SMPS



TOLL

NOTE:
 LOGO - GS
 GMXXXX- Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

General Information

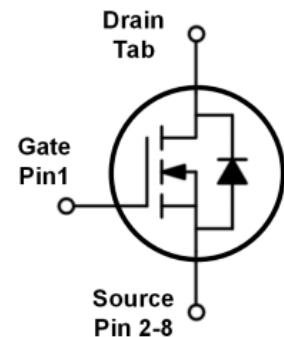
Shipping

- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

Equivalent circuit



Absolute maximum rating@25°C

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	200	V
Gate-source voltage	V_{GS}	±20	
Continuous drain current	I_D	$T_C=25^\circ C$ ⁽¹⁾	61
		$T_C=100^\circ C$	43
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	244	A
Avalanche energy, single pulse ⁽³⁾	E_{AS}	542	mJ
Power dissipation	P_D	$T_C=25^\circ C$	254
		$T_A=25^\circ C$ ⁽⁴⁾	127
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	°C

Thermal Characteristic

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	0.59	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	$R_{\theta JA}$	35	

**Electrical Characteristics (T_J=25°C unless otherwise noted)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0, I _D = 250 μA	200			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5	3.4	4.5	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		20.6	22	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 20 A		40		S
Gate resistance	R _g	f = 1 MHz		2.5		Ω
Dynamic ⁽⁵⁾						
Total gate charge V _{GS} = 10 V	Q _g	V _{DS} = 100 V, I _D = 20 A, V _{GS} = 10 V		35		nC
Gate-source charge	Q _{gs}			11.5		
Gate-drain charge	Q _{gd}			7.5		
Turn-on delay time	t _{d(on)}	V _{DS} = 100 V, I _D = 20 A, V _{GS} = 10 V, R _{GEN} = 3 Ω		8.6		ns
Rise time	t _r			17		
Turn-off delay time	t _{d(off)}			28		
Fall time	t _f			22		
Input capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		2363		pF
Output capacitance	C _{oss}			184		
Reverse transfer capacitance	C _{rss}			12.1		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 2 A		0.7	1.2	V
Reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs		100		ns
Reverse recovery charge	Q _{rr}				419	

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) V_{DS} = 100 V, V_{GS} = 10 V, L = 1.0 mH.
- (4) Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
- (5) Guaranteed by design, not subject to production testing.



Typical Performance Characteristics

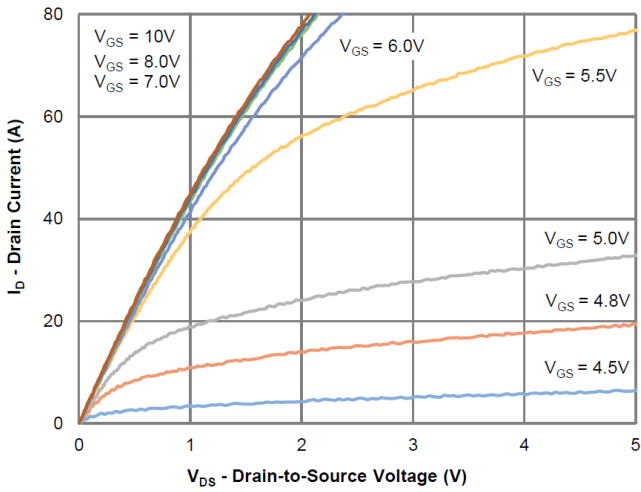


Figure 1: Output Characteristics

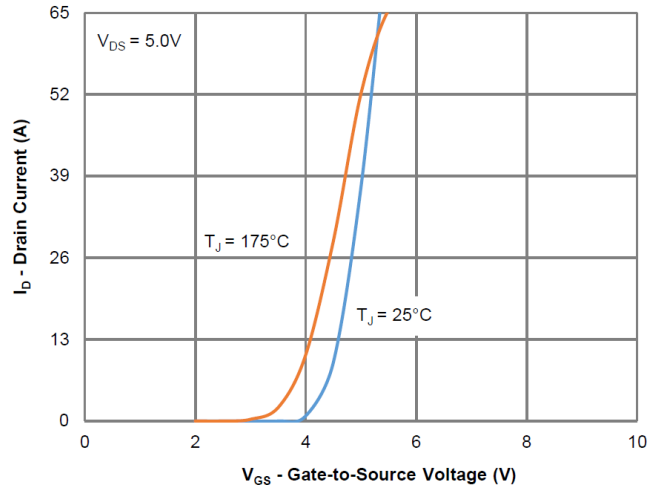


Figure 2: Transfer Characteristics

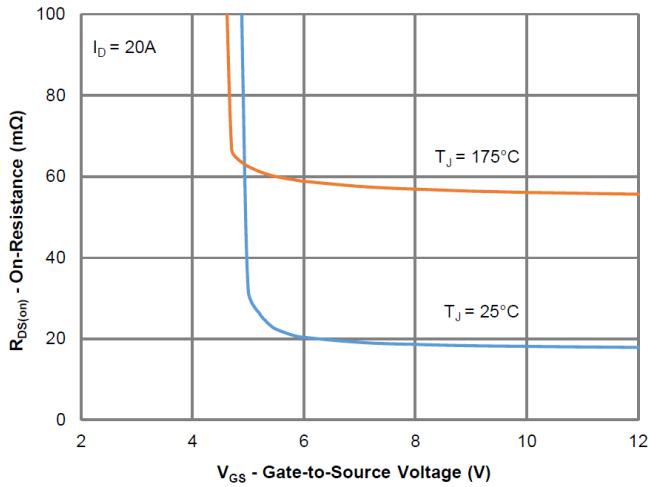


Figure 3: On-Resistance vs. Gate-Source Voltage

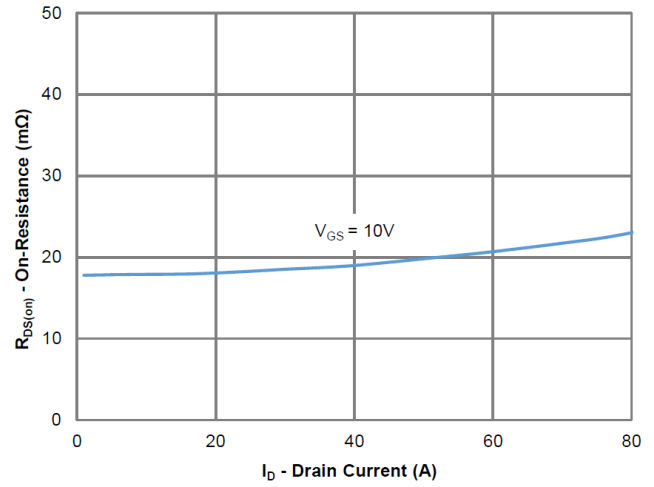


Figure 4: On-Resistance vs. Drain Current

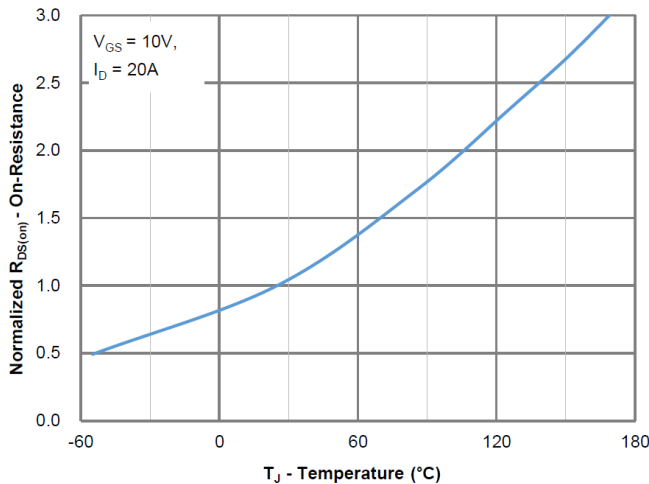


Figure 5: On-Resistance vs. Junction Temperature

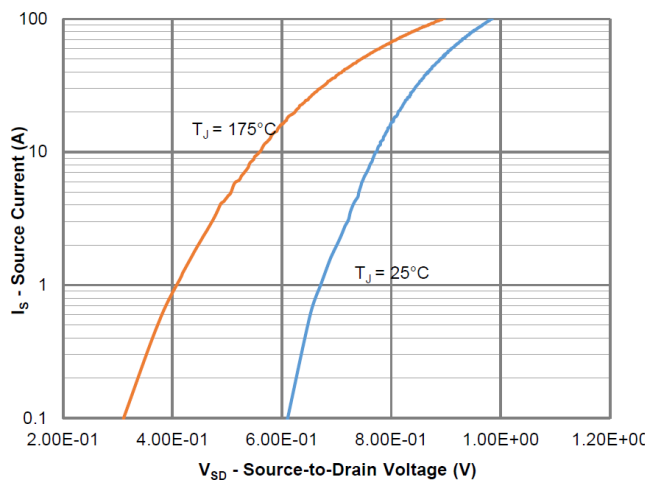


Figure 6: Source-Drain Diode Forward Voltage



Typical Performance Characteristics

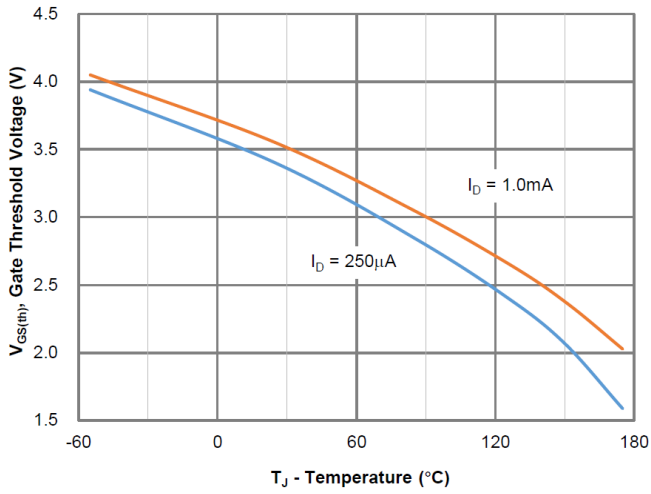


Figure 7: Gate Threshold Variation vs. Junction Temperature

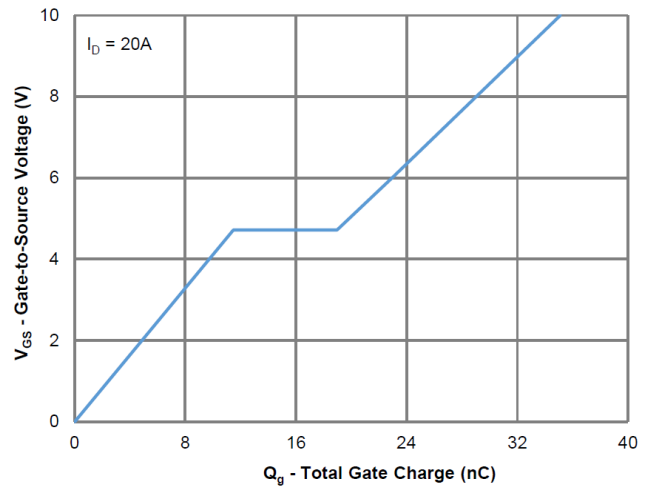


Figure 8: Gate Charge Characteristics

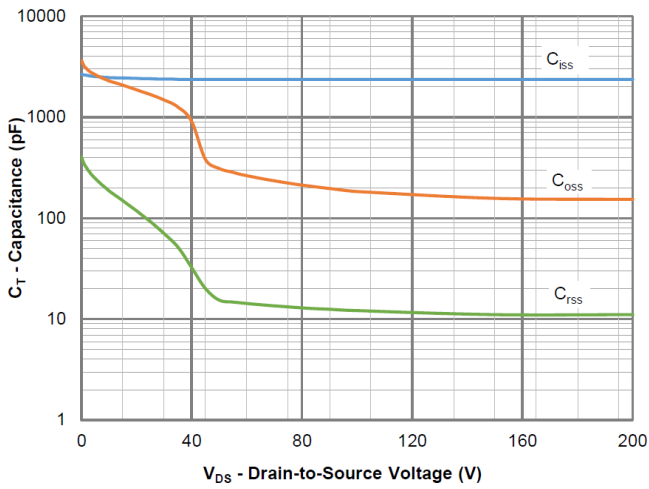


Figure 9: Capacitance Characteristics

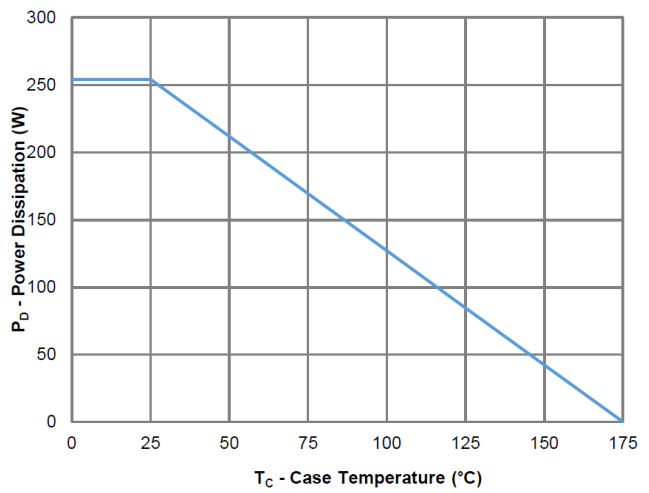


Figure 10: Power Derating

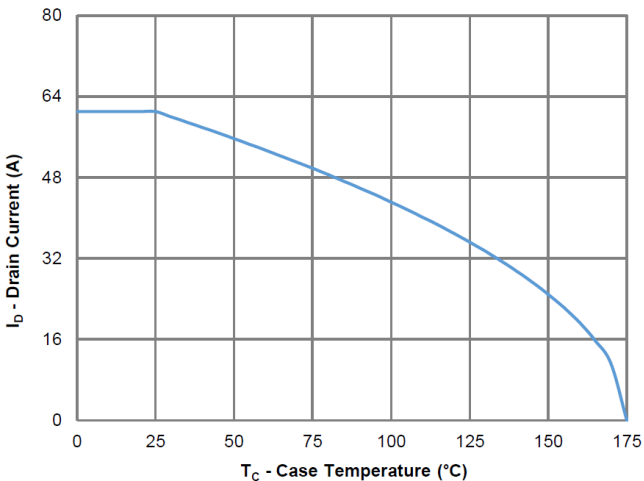


Figure 11: Current Derating

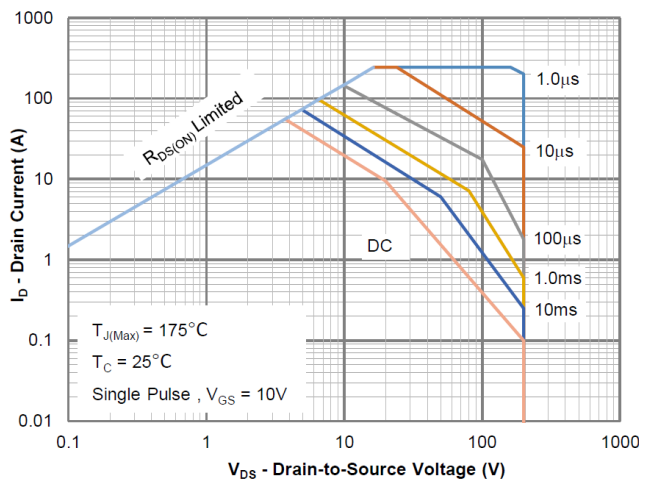


Figure 12: Safe Operating Area



Typical Performance Characteristics

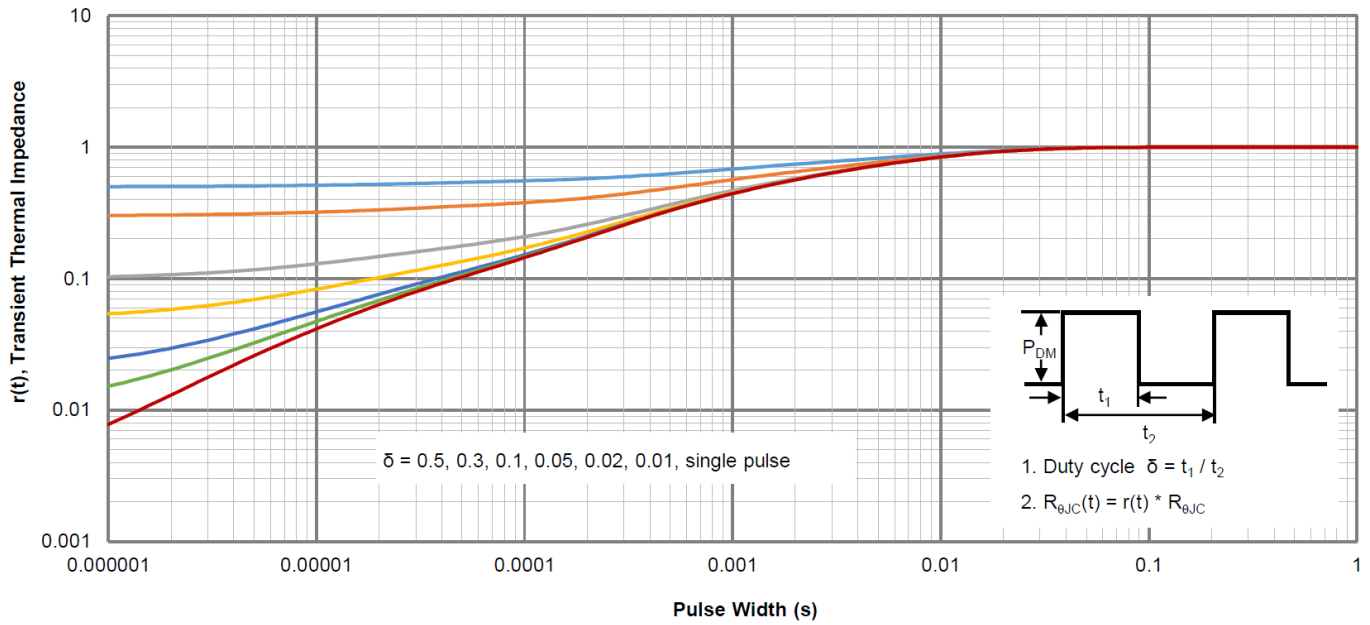
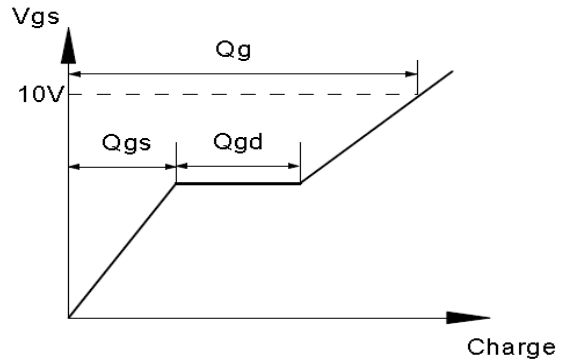
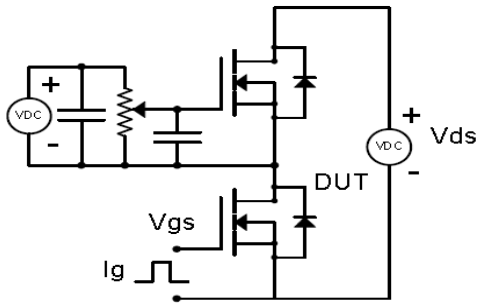


Figure 13: Normalized Maximum Transient Thermal Impedance

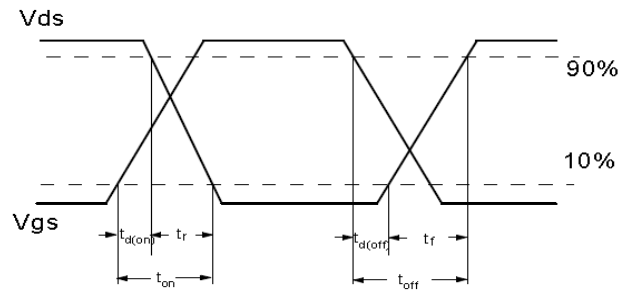
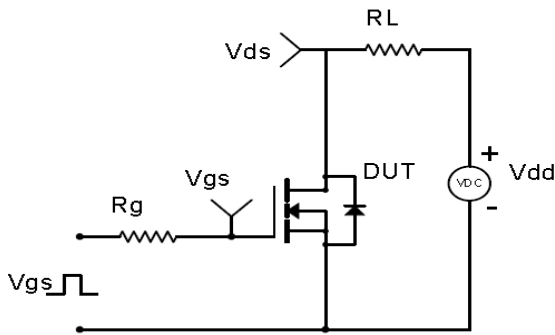


Test Circuit & Waveform

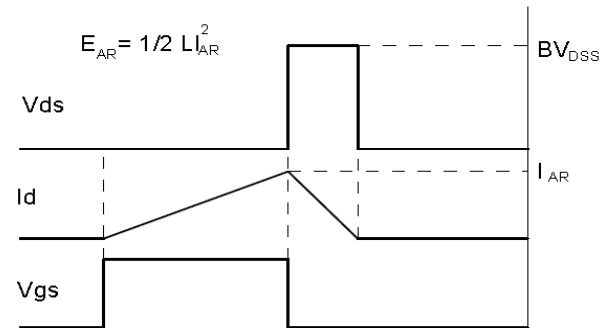
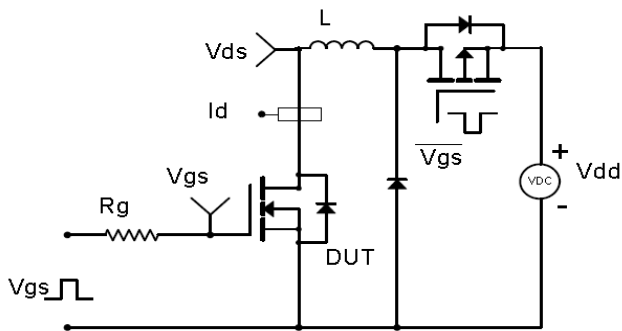
Gate Charge Test Circuit & Waveform



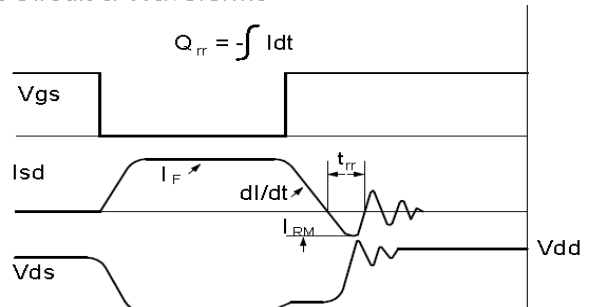
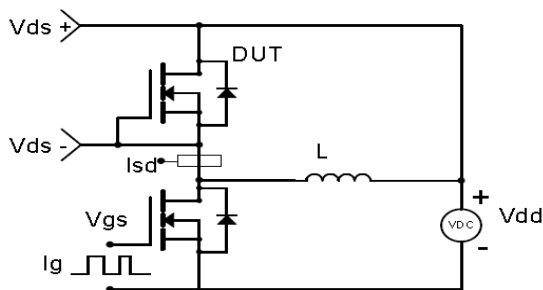
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

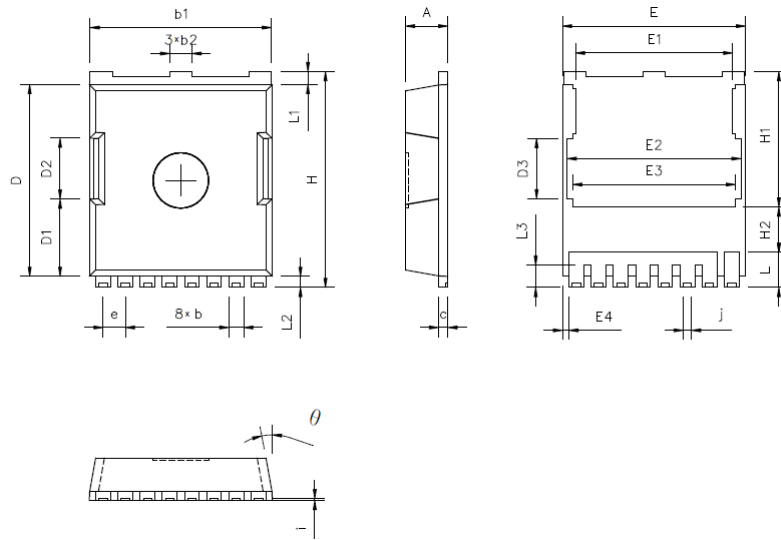


Diode Recovery Test Circuit & Waveforms





Package outline dimensions: TOLL



Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
θ	10° REF		

Important Notice

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Gostone reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Gostone or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Gostone in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Gostone or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. In addition, any recipient of this document and the relevant products samples may not alter, decompile, disassemble, reverse engineer, or otherwise modify any information/samples received hereunder. Any intellectual property rights arising from the reverse engineering of Gostone's products shall belong to Gostone.