

GMS160N20L3

## N-Channel 200V,16mΩ max,SGT Power MOSFET

# **Product Summary**

V <sub>DS</sub> (V)	$R_{DS(on),max}$ (m $\Omega$ )	I <sub>D</sub> (A)
200	16 @ V <sub>GS</sub> = 10V	81 <sup>(1)</sup>

#### **Features**

- Low R<sub>DS(on)</sub> SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

### **Application**

- DC/DC conversion
- Power switch
- Synchronous Rectification in SMPS

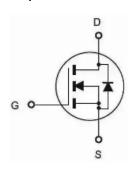


# **GMXXXX** GS **FAYWWLT**

TO-263

NOTE: LOGO - GS GMXXXXX- Part number code F - Fab location code A - Assembly location code Y - Year code WW - Week code L&T - Assembly lot code

#### **Equivalent circuit**



# Absolute maximum rating@25℃

Parameter			Limit	Unit
Drain-source voltage			200	V
Gate-source voltage			±20	
	T <sub>C</sub> =25°C <sup>(1)</sup>		81	А
Continuous drain current	Tc=100°C	l <sub>D</sub>	58	
Pulsed drain current <sup>(2)</sup>			326	
Avalanche energy, single pulse <sup>(3)</sup>			922	mJ
Down discipation	T <sub>C</sub> =25°C	- P <sub>D</sub>	288	W
Power dissipation	T <sub>A</sub> =25°C <sup>(4)</sup>		144	
Operating junction and storage temperature range			-55 to 150	°C

#### **Thermal Characteristic**

Parameter	Symbol	Max.	Unit	
Thermal resistance, junction-to-case	Steady state	Rejc	0.52	°C/W
Thermal resistance, junction-to-ambient (4)	Steady state	Reja	33	C/VV



## **Electrical Characteristics (TJ=25** °C unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Тур.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ , $I_D = 250 \mu A$	200			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, \ I_D = 250 \ \mu A$	2.5	3.4	4.5	V
Gate-body leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μΑ
Drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		13.6	16	mΩ
Forward transconductance (5)	g <sub>fs</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 50 A		38		S
Gate resistance	Rg	f = 1 MHz		2.5		Ω
Dynamic (5)						
Total gate charge V <sub>GS</sub> = 10 V	$Q_g$			31		nC
Gate-source charge	$Q_gs$	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V		9.8		
Gate-drain charge	$Q_{gd}$			7.7		
Turn-on delay time	t <sub>d(on)</sub>			14		
Rise time	tr	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10		16		
Turn-off delay time	t <sub>d(off)</sub>	V, R <sub>GEN</sub> = 3 Ω		28		ns
Fall time	t <sub>f</sub>			12		
Input capacitance	C <sub>iss</sub>			2050		
Output capacitance	$C_{oss}$	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz		297		pF
Reverse transfer capacitance	$C_{rss}$			11		
Reverse Diode Characteristics (5)						
Diode forward voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 2 A		0.7	1.2	V
Reverse recovery time	t <sub>rr</sub>	1 - 20 A dildt - 400 A/v-		120		ns
Reverse recovery charge	Qrr	I <sub>F</sub> = 20 A, di/dt = 100 A/μs		524		nC

#### Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3)  $V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, L = 1.0 \text{ mH}.$
- (4) Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
- (5) Guaranteed by design, not subject to production testing.



## **Typical Performance Characteristics**

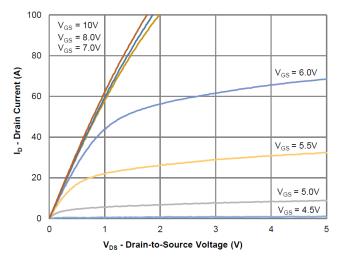


Figure 1: Output Characteristics

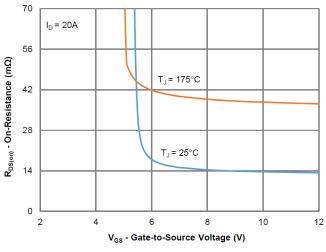


Figure 3: On-Resistance vs. Gate-Source Voltage

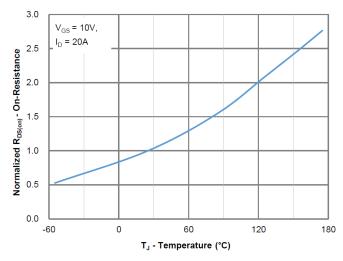


Figure 5: On-Resistance vs. Junction Temperature

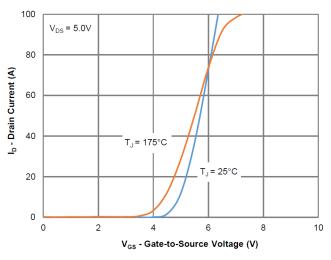


Figure 2: Transfer Characteristics

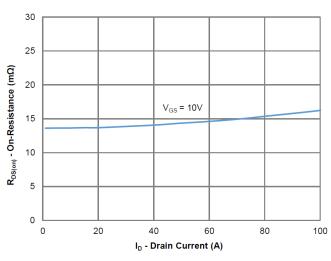


Figure 4: On-Resistance vs. Gate-Source Voltage

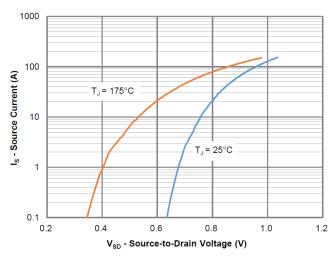


Figure 6: Source-Drain Diode Forward Voltage



# Typical Performance Characteristics

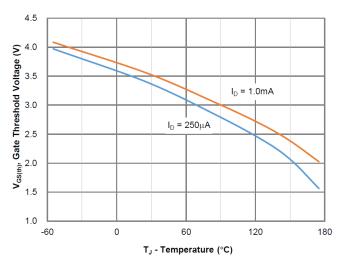


Figure 7: Gate Threshold Variation vs. Junction Temperature

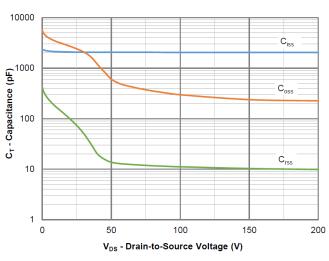


Figure 9: Capacitance Characteristics

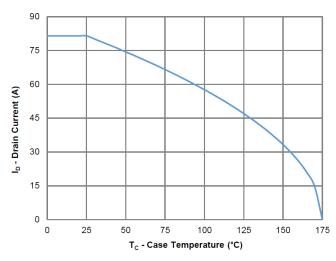


Figure 11: Current Derating

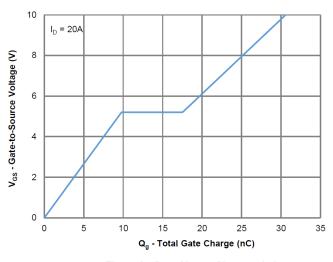


Figure 8: Gate Charge Characteristics

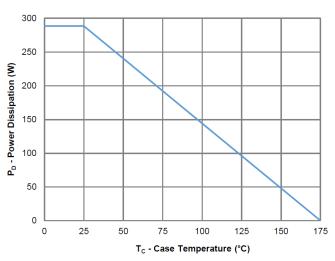


Figure 10: Power Derating

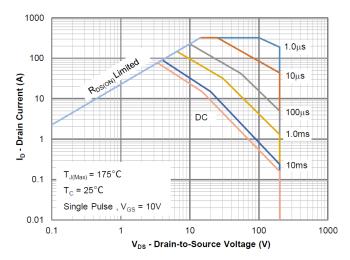


Figure 12: Safe Operating Area



# Typical Performance Characteristics

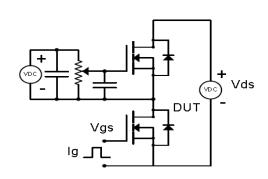


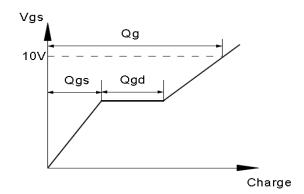
Figure 13: Normalized Maximum Transient Thermal Impedance



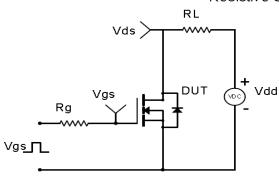
## **Test Circuit & Waveform**

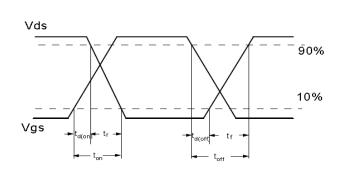
#### Gate Charge Test Circuit & Waveform



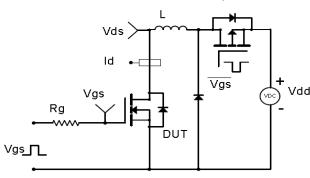


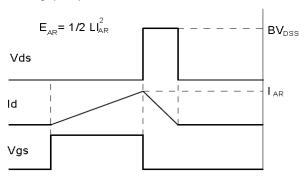
Resistive Switching Test Circuit & Waveforms



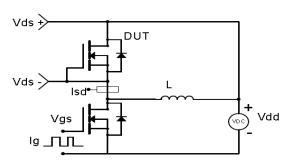


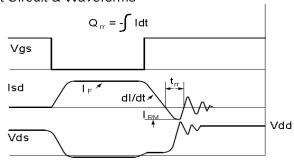
#### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





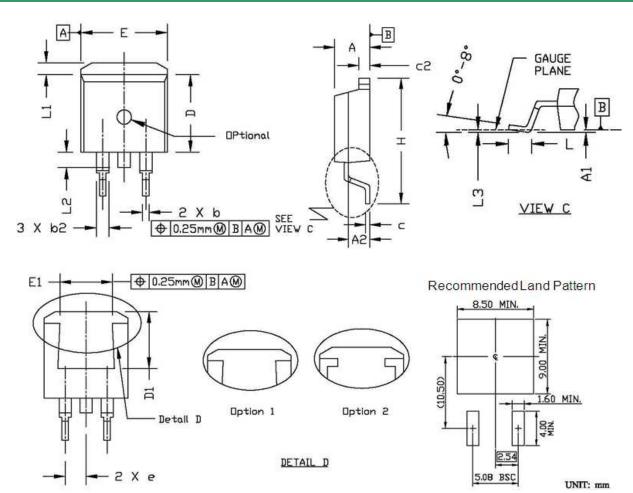
#### Diode Recovery Test Circuit & Waveforms







## **Outline Drawing TO-263**



Cymahal	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	4.30	4.86	0.169	0.191	
A1	0.00	0.25	0.000	0.010	
A2	2.34	2.79	0.092	0.110	
b	0.68	0.94	0.027	0.037	
b2	1.15	1.35	0.045	0.053	
С	0.33	0.65	0.013	0.026	
c2	1.17	1.40	0.046	0.055	
D	8.38	9.45	0.330	0.372	
D1	6.90	8.17	0.272	0.322	
е	2.54 BSC.		0.100 BSC.		
E	9.78	10.50	0.385	0.413	
E1	6.50	8.60	0.256	0.339	
Н	14.61	15.88	0.575	0.625	
L	2.24	3.00	0.088	0.118	
L1	0.70	1.60	0.028	0.063	
L2	1.00	1.78	0.039	0.070	
L3	0.00	0.25	0.000	0.010	



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