

Product Summary

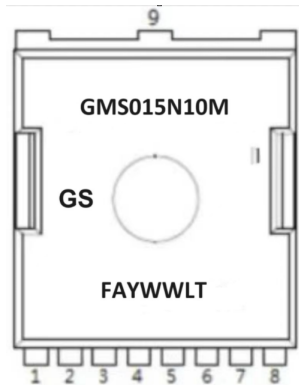
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
100	1.5 @ $V_{GS} = 10V$	330 ⁽¹⁾

Features

- ❖ Low $R_{DS(on)}$
- ❖ Trench power MOSFET
- ❖ Low Gate Charge

Application

- ❖ Stored energy
- ❖ Electric motorcycle



TOLL

NOTE:
 LOGO - GS
 GMS015N10M - Part number code
 F - Fab location code
 A - Assembly location code
 Y - Year code
 WW - Week code
 L&T - Assembly lot code

General Information

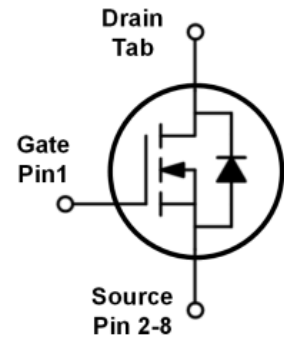
Shipping

- ❖ One shipping options is offered as standard
- ❖ Un-sawn wafer

Handling

- ❖ Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- ❖ Product must be handled only in a class 10,000 or better-designated clean room environmen

Equivalent circuit



Absolute Maximum Rating ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	$T_C=25^\circ\text{C}$ ⁽¹⁾	I_D	A
	$T_C=100^\circ\text{C}$	330 246	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	1320	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	1750	mJ
Power dissipation	$T_C=25^\circ\text{C}$	P_D	431 W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Characteristic ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Max.	Unit
Thermal resistance, junction-to-case	$R_{\theta JC}$	0.29	$^\circ\text{C/W}$
Thermal resistance, junction-to-ambient ⁽⁴⁾	$R_{\theta JA}$	40	

**Electrical characteristics (Ta=25°C ± 3°C)**

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	100			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.2	3	3.8	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 100 A		1.18	1.5	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 100 A		280		S
Gate resistance	R _g	f = 1 MHz, open drain		1	2	Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 50 V, I _D = 100 A, V _{GS} = 10 V		258	362	nC
Gate-source charge	Q _{gs}			68	96	
Gate-drain charge	Q _{gd}			74	104	
Turn-on delay time	t _{d(on)}	V _{DS} = 50 V, I _D = 100 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		64	128	ns
Rise time	t _r			61	122	
Turn-off delay time	t _{d(off)}			221	442	
Fall time	t _f			104	208	
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		15650	21910	pF
Output capacitance	C _{oss}			2100	2940	
Reverse transfer capacitance	C _{rss}			45	90	
Reverse Diode Characteristics(5)						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 100 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 50 V, I _F = 100 A, di/dt = 100 A/μs		126	227	ns
Reverse recovery charge	Q _{rr}			427	769	nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, L = 0.3\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

Electrical characteristics diagrams

Fig.1 Typ. transfer characteristics

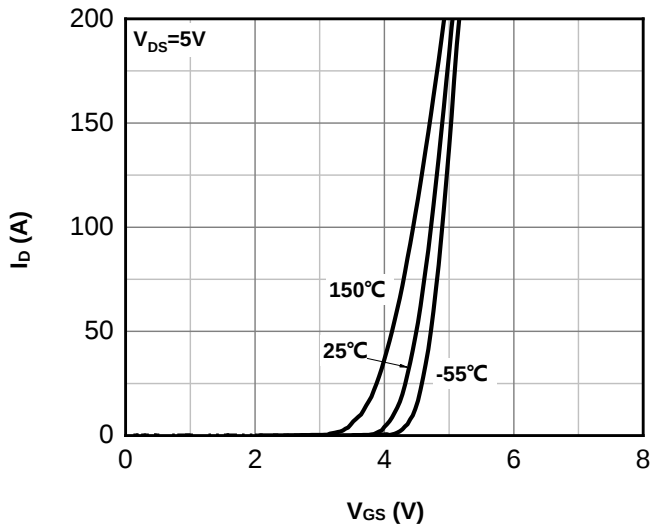


Fig.2 Typ. output characteristics

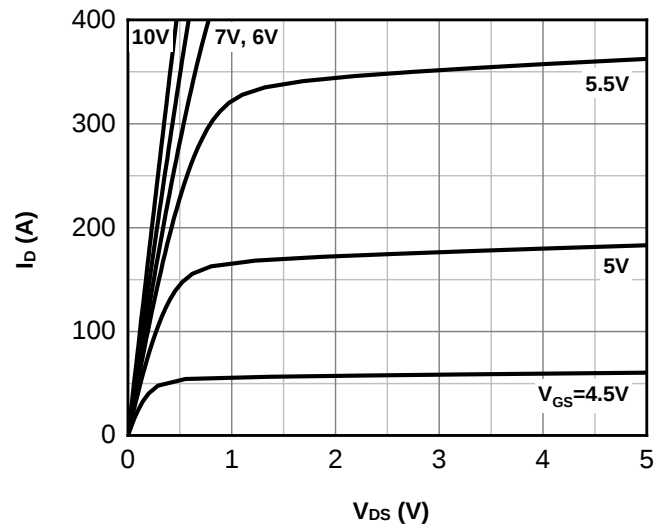


Fig.3 Normalized on-resistance vs drain current

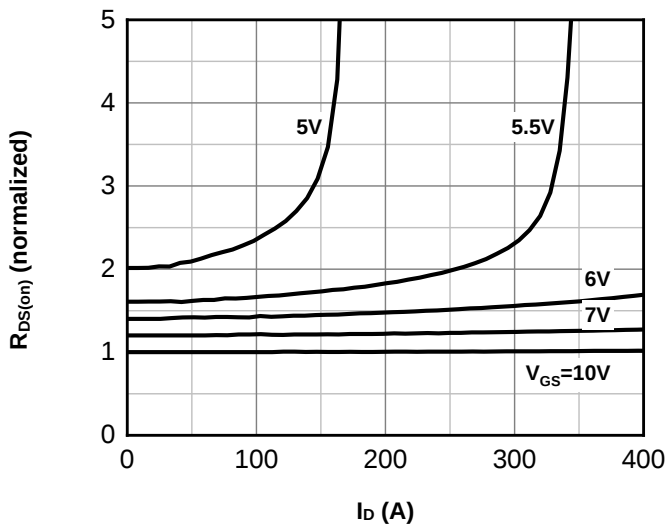


Fig.4 Typ. on-resistance vs gate-source voltage

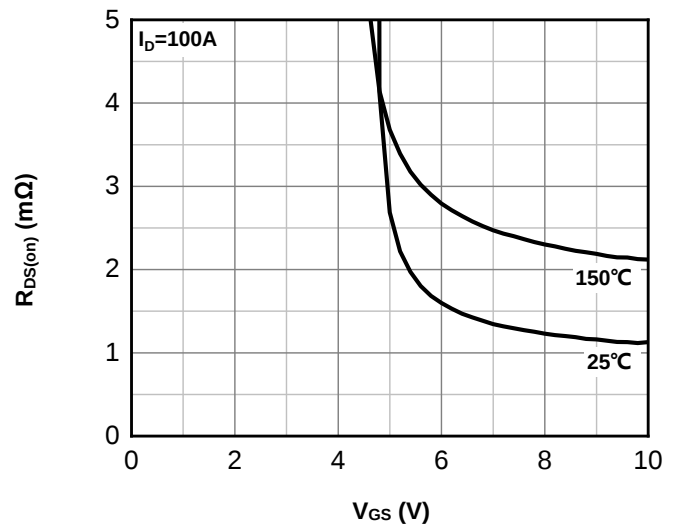


Fig.5 Normalized on-resistance vs junction temperature

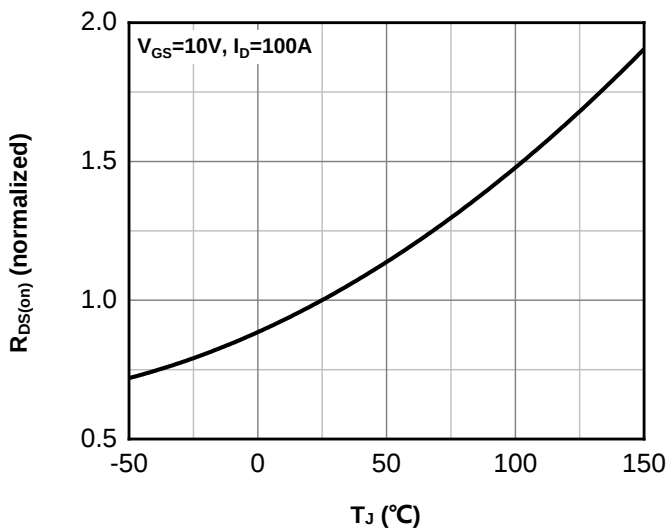
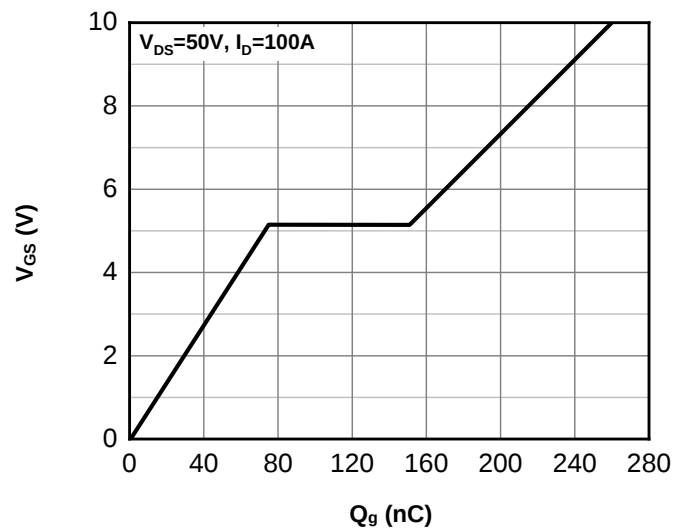


Fig.6 Typ. gate charge



Electrical characteristics diagrams

Fig.7 Typ. forward characteristics of body diode

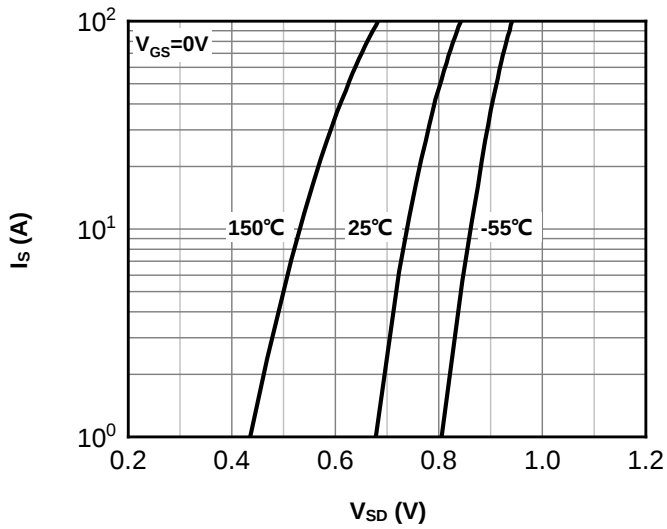


Fig.8 Safe operating area

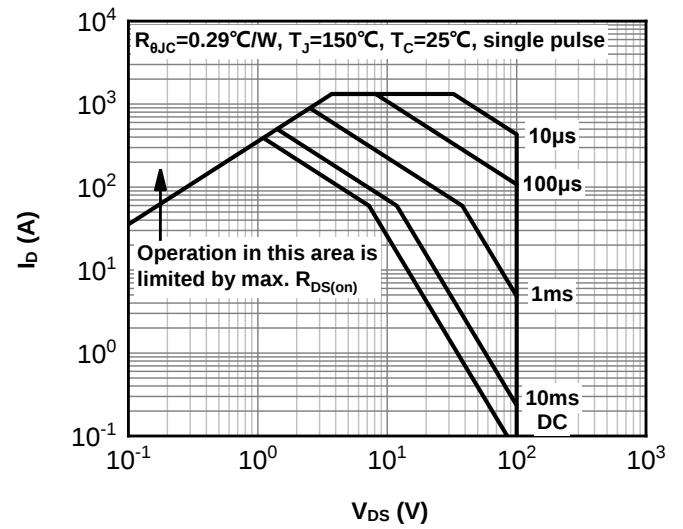


Fig.9 Typ. Capacitance

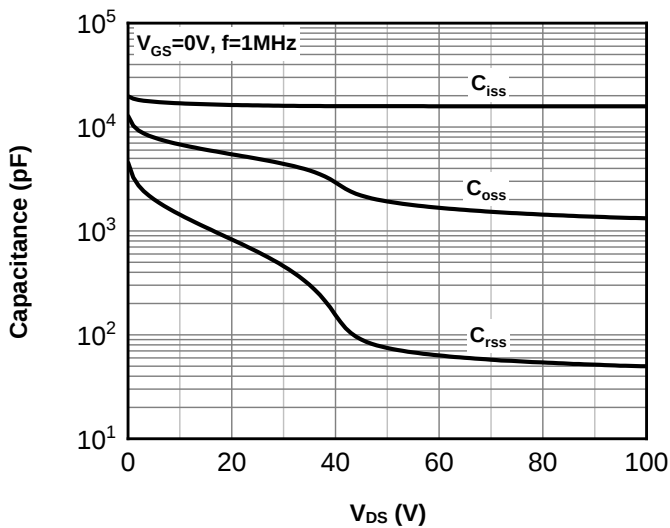


Fig.10 Single pulse maximum power dissipation

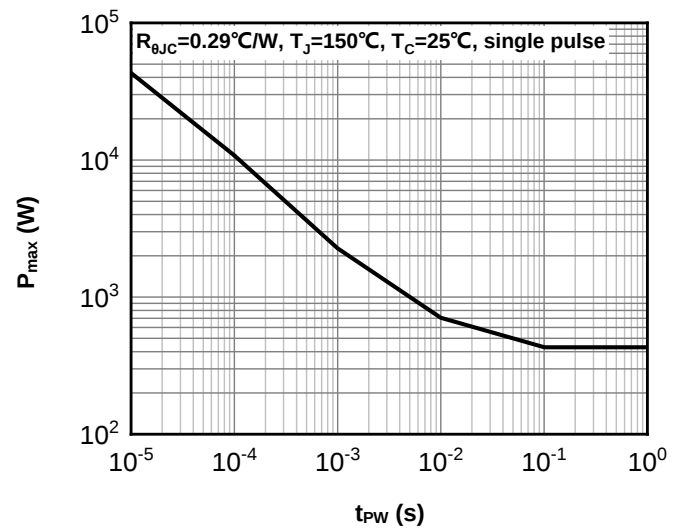


Fig.11 Max. power dissipation vs case temperature

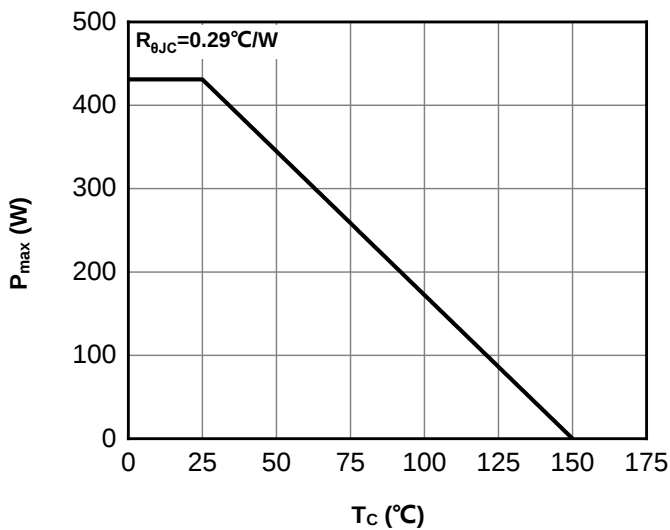
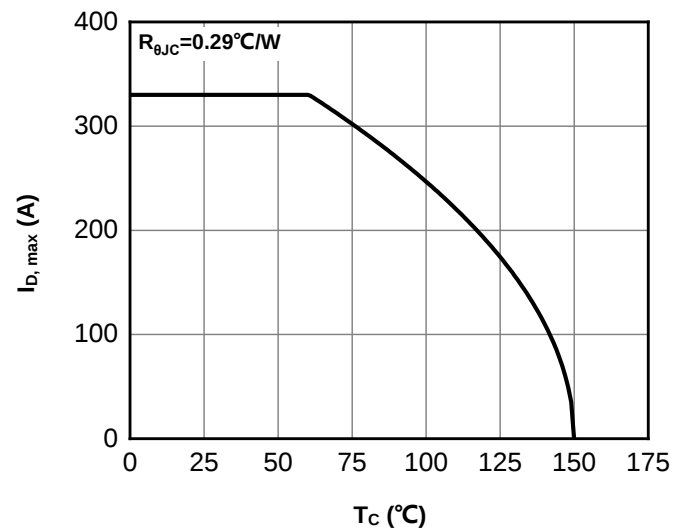


Fig.12 Max. continuous drain current vs case temperature



Electrical characteristics diagrams

Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

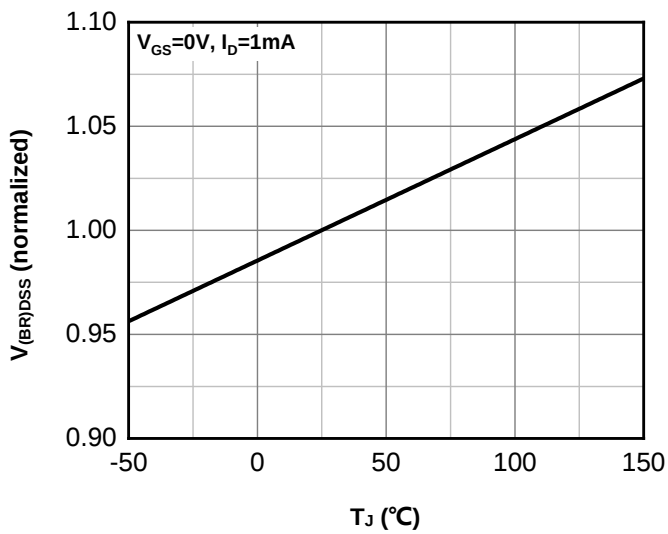


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

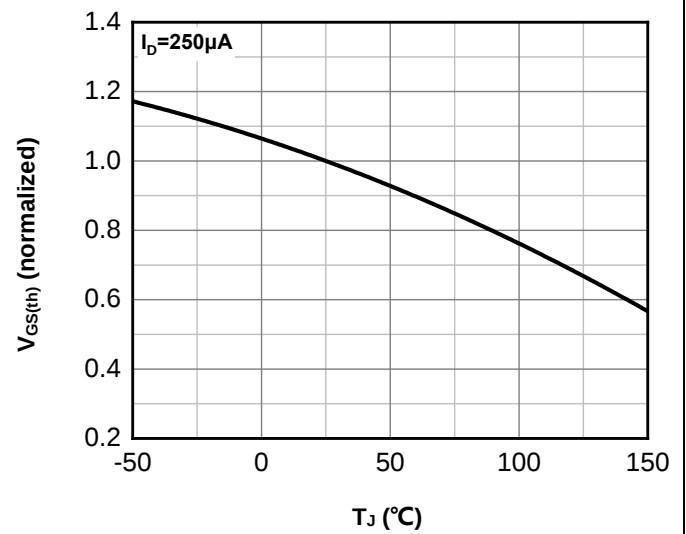
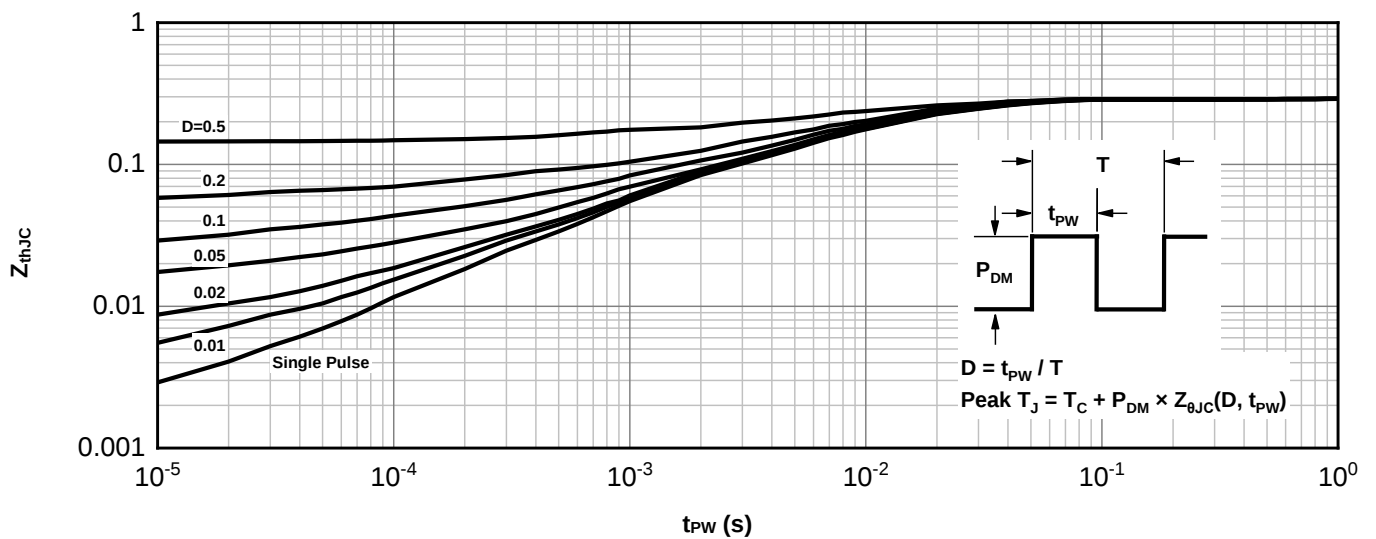
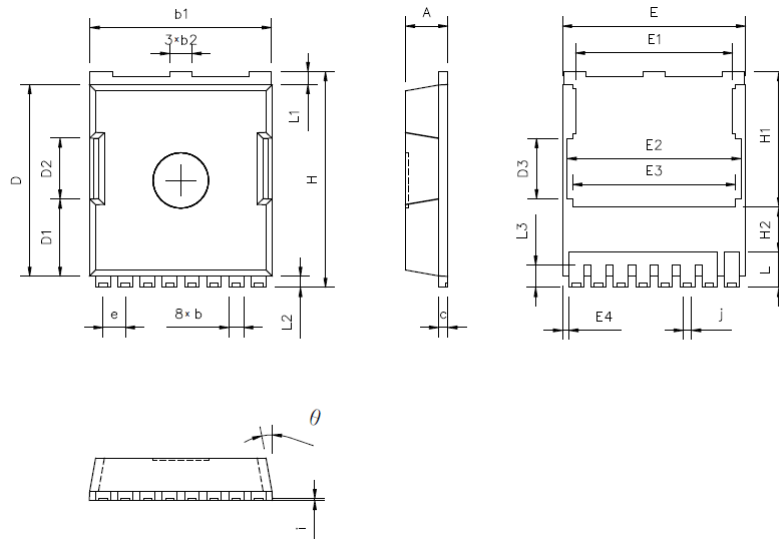


Fig.15 Transient thermal impedance from junction to case



Package outline dimensions: TOLL


Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
θ	10° REF		

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